A 1.1 mW 60 dB dynamic range Received Signal Strength Indicator with low power Limiting Amplifier

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Abstract: A low-power CMOS limiting amplifier (LA) and received signal strength indicator (RSSI) are presented. The proposed LA employs folded diode structure with source degeneration load. This structure requires less transconductance than that of conventional structure. The proposed RSSI consists of seven stage of LA, full wave rectifier (FWR), and second order LPF. The RSSI is designed using 0.18 µm CMOS technology. It shows 60 dB input dynamic range and power consumption is 1.1 mW on the 1.8 V supply. Nominal slope of the RSSI transfer curve is 20 mV / dB at 20 kΩ load.

1. Introduction

Wireless devices market demands on long battery life and high performance. Fig. 1 shows the conventional direct conversion wireless receiver. This consists of low noise amplifier (LNA), mixer, voltage controlled oscillator (VCO), low pass filter (LPF), variable gain amplifier (VGA) and RSSI.

Fig. 2 shows the block diagram of RSSI. It consists of LAs, FWRs, and LPF. The output signal of mixer is entered into the RSSI input. This signal is amplified through LA. Each output voltage of LA is rectified and converted to current at FWR. The signal of RSSI_out in Fig. 2 is obtained by summing all FWR current output into an external resistor $R_1$. The output second order filter reduces ripple. Then the amplified signals provide arithmetic increment at the RSSI_out in dB scale. RSSI normally represent received signal strength by DC voltage. It can also be used to adjust signal overall gain and control receiver power management. LA is the critical block of the RSSI power consumption. Decreasing LA power consumption is decreasing total power consumption of RSSI.

In this paper we have designed low power RSSI using proposed LA with source degeneration load. RSSI sub-block and proposed low power LA are described in section 2. The simulation results are presented in section 3. Finally, the conclusion is drawn in section 4.

2. RSSI Design

Fig. 2 shows the general block diagram of RSSI. This block consists of LA, FWR, and LPF. For logarithmic detection of input signal the LA is configured of cascade structure. The LA consists of $N$ identical gain stage. Single stage gain $A_S$ and 3-dB bandwidth $f_S$ was derived as [1]

$$A_S = A_s^{(U/N)}$$  \hspace{1cm} (1)

Fig. 3 (a) shows conventional folded diode connected LA. Conventional LA voltage gain is [1]

$$f_s = \frac{f_f}{\sqrt{2V_N^2 - 1}}$$  \hspace{1cm} (2)

where $A_s$ and $f_f$ are overall gain and bandwidth of the limiting amplifier, respectively and $N$ is number of stage. Number of LA stage is decided in consideration of RSSI maximum gain error [1]. The maximum error compared with the ideal logarithmic curve can be derived as [1]:

$$Error_{max}(dB) = 10((-1 + \sqrt{A_s + A_f})\log A_s - (A_s - 1)\log(4 + (2A_s - 2))/A_s - 1)$$  \hspace{1cm} (3)

The 9 dB of voltage gain of each stage is obtained by using seven stages of LA in the RSSI. Overall LA gain is more than 60 dB. The RSSI maximum error is smaller than ±1 dB.

2.1 Low Power Limiting Amplifier

The Fig. 3 (a) shows conventional folded diode connected LA. Conventional LA voltage gain is [1]

$$A_s = G_mR_{out} = g_m\times1/G_m$$  \hspace{1cm} (4)

where $g_m$ is the transconductance of the corresponding device $M_{cm}$. This type of LA is used for low voltage operation. The voltage gain of this structure is 9.5 dB. The drain current of $Mn4$ and $Mn1$ are 16.9 μA and 24.5 μA, respectively.
The proposed LA structure is shown in Fig. 3. The voltage gain of this LA is derived as

$$A_v = g_{m_{mn1}} \times \left( \frac{1}{g_{m_{mn4}}} + R_s \right)$$

(5)

The source degeneration resistor is used in this proposed structure to increase the output load resistance, which decreases the transconductance of the input transistor under fixed gain. This structure decreases the total power consumption.

The effective output impedance of the proposed LA is calculated using equivalent circuit model of the source degeneration load. Fig. 4 shows output load and equivalent circuit model of the proposed source degeneration. It can be derived

$$I_s = g_m \left( V_x - I_s R_s \right) + \frac{V_x - I_s R_s}{r_o}$$

(6)

$$Z_{out} = \frac{1}{I_x} = \frac{1}{g_m} + R_s$$

(7)

Figure 3. The schematic of (a) conventional folded diode connected limiting amplifier (b) proposed limiting amplifier.

Figure 4. The source degeneration load (a) schematic (b) equivalent circuit model.

Fig. 5 is the full schematic with common mode feedback and the voltage transfer curve of the proposed LA. Table 1 shows the simulation results of conventional and proposed LA. It is shown that proposed LA has less power consumption.

Figure 5. The proposed LA (a) full schematic (b) voltage transfer curve
Table 1. Comparison LA

<table>
<thead>
<tr>
<th></th>
<th>Proposed LA</th>
<th>Conventional LA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.8 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>9.5 dB</td>
<td>9.5 dB</td>
</tr>
<tr>
<td>THD</td>
<td>1.16 %</td>
<td>1.16 %</td>
</tr>
<tr>
<td>Total current</td>
<td>53.6 uA</td>
<td>98.3 uA</td>
</tr>
</tbody>
</table>

2.2 Full Wave Rectifier

Fig. 6 shows schematics of conceptual and realized FWR [2]. Fig. 6 (a) shows a half-wave rectifier. \( M_{nf} \) and \( M_{pf} \) are turned on and off, respectively, depending on the direction of input current \( I_{in} \).

Figure 7. when the input voltage is \( 2 \, mV_{pp} \), transient response each state of (a) LA output voltage (b) FWR output current.

Then a half-wave rectified output current \( I_{rec} \) flows at output. Therefore, the full-wave rectifier can be designed by utilizing two half-wave rectifier in parallel. Fig. 6 (b) is the schematic of the FWR [3]. This type is current mode rectifier. It consists of transconductance stage and current mode FWR. This FWR employs two additional techniques. One is that nMOS is used instead of pMOS. The pMOS \( M_{pf} \) is replayed by \( M_{pf1} \) and diode connection \( M_{nf2} \). This “nMOS substitute” improves the speed. The other technique is “the pre-bias method”. The \( V_{bs} \) in the Fig. 6 (a) biases two switches at the nearly-on condition. This condition makes the switch fully ON and OFF by small amount of input current. \( M_{nf1} \) and \( M_{nf3} \) are transconductance stages that convert input voltage to current. Transistor pairs \( M_{nf2} \), \( M_{nf6} \) and \( M_{nf4} \), \( M_{nf5} \) are turned on alternatively. The rectified current at output of each current mode FWR is summed in second-order filter. The filter converts current to voltage and does noise filtering. The RSSI output level is adjusted with external second order filter.

3. Simulation Results

The proposed RSSI has been optimized and simulated using 0.18 \( \mu m \) standard CMOS process. The total power consumption is 1.1 \( mW \) at a 1.8 \( V \) supply voltage. Fig. 7 shows transient response of the proposed low power LA output voltage and of the FWR output current. Simulated LA gain is 9.5 \( dB \).

The RSSI input vs. output transfer curve are shown in Fig. 8. Proposed RSSI has 7 stage LAs, 7 stage FWRs, and second-order filter. The dynamic range of the RSSI is 60dB(from -80 \( dBm \) to -20 \( dBm \)) on the supply voltage of 1.8 \( V \), and power consumption is approximately 1.1 \( mW \). Nominal slope of the RSSI transfer curve is 20 \( mV/dB @ 20 \, k\Omega \) load. The proposed RSSI is 35% more power efficient than a conventional RSSI.
Figure 8. RSSI transfer curve.

Table 2 shows summaries of simulation results of proposed RSSI (with proposed low power LA) performance and comparison of the conventional (with conventional LA).

Table 2. Performance summaries of the proposed RSSI

<table>
<thead>
<tr>
<th></th>
<th>Conventional</th>
<th>Proposed</th>
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<tbody>
<tr>
<td>Technology</td>
<td>0.18 μm CMOS</td>
<td></td>
</tr>
<tr>
<td>Limiting Amplifier</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single stage gain</td>
<td>9.5 dB</td>
<td></td>
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<tr>
<td>Input dynamic range</td>
<td>±125 mV</td>
<td>±300 mV</td>
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<tr>
<td>Total Harmonic Distortion</td>
<td>1.16 %</td>
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<tr>
<td>Power consumption</td>
<td>176.9 µW</td>
<td>96.5 µW</td>
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<tr>
<td>RSSI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RSSI dynamic range</td>
<td>60 dB (-80 dBm ~ -20 dBm)</td>
<td></td>
</tr>
<tr>
<td>Nominal slope</td>
<td>20 mV / dB (@ 20 kΩ load)</td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.8 V</td>
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<tr>
<td>Total Consumption</td>
<td>1.67 mW</td>
<td>1.1 mW</td>
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</table>

4. Conclusion

RSSI using low power LA is proposed in this paper. The low power LA employs folded diode structure with source degeneration load. This structure demands less transconductance than conventional structure.

It is simulated using 0.18 μm CMOS technology. The dynamic range of the RSSI is 60 dB (from -80 dBm to -20 dBm) on the supply voltage of 1.8 V, and total power consumption is approximately 1.1 mW. Nominal slope of the RSSI transfer curve is 20 mV / dB @ 20 kΩ load. The proposed RSSI is 35% more power efficient than a conventional RSSI. It is adoptable to low power solution.

Acknowledgment

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References