GPU Acceleration of an FDTD Solver for MMIC Passive Element Analysis

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Abstract—GPU acceleration algorithm for an FDTD solver of analyzing MMIC passive element circuit characteristics is presented. Lines having the input or output ports are assumed to be microstrip lines. The analysis region is surrounded by a CFSPML absorbing boundary region. Not only the fields in the absorbing boundaries, and voltages and currents at the ports, but also field distributions in a plane are computed by using the GPU device, thus the speedup rate compared with GPU-less computation is more than a factor of 10 under the circumstances of one Tesla 2075 GPU and two Intel Xeon(R) E5620 CPU (total 8 cores).

I. INTRODUCTION

The power of GPU (Graphics Processing Unit) acceleration has been fully demonstrated in a broad range of scientific and engineering computer simulation [1]. Recently, in the area of electromagnetic simulation also, the subjects on GPU acceleration have come to attract considerable attention of many researchers and engineers [2]-[6]. The FDTD analysis looks very suitable to GPU calculation, because both are fit for parallel processing. However, it is not so easy to make the best use of GPGPU (General Purpose computing on GPU) techniques to practical problems involving many complicate calculation processes other than basic FDTD equations.

This paper presents GPU acceleration algorithm for the problem comprising considerably complex calculation processes, i.e., that of obtaining MMIC passive element circuit characteristics after FDTD calculation of fields being completed for the regions surrounded by CFSPML (Complex Frequency Shifted Perfectly Matched Layer) absorbing boundaries. The algorithm here includes, in addition to calculation of S parameters, calculation of field distributions in a plane without deterioration of speed, which has not been considered in the past work [7].

II. ANALYSIS OF MMIC PASSIVE ELEMENTS

A. Geometry of the Problem

MMIC passive elements considered here are of the structure in which various shapes of strip conductors are positioned on the upper surface of the dielectric substrate backed underneath with a ground conductor. All input and output ports are placed on MSLs (Microstrip lines). Calculation region is of a cuboid shape surrounded the upper and lateral sides by PML regions.

B. Input and Output Ports

Excitation is given by a pulsed wave being added for vertical electric field components positioned on the rectangular vertical plane underneath the microstrip signal conductor. The same shape of pulsed wave is also given for the horizontal magnetic field components on the neighbouring rectangular vertical plane in such a way that the phase and amplitude of magnetic fields fulfil one-way traveling plane wave condition together with the associated electric field components. Input port position is placed at about a quarter wavelength apart from the excitation position, aiming at having good propagation mode field distribution at the input port. Output ports are taken at about several to ten FDTD cell widths apart from circuit element edges and PML regions.

C. Calculation of S Parameters

To maintain high accuracy analysis, S parameters are not calculated from port voltages only but from port voltages, port currents, and those characteristic impedances of MSL which are calculated separately from FDTD analysis of the corresponding straight MSL.

D. FDTD mesh arrangements

FDTD mesh division scheme is determined based on edge positions of the input port MSL. Namely, the electric field located lines are set at the positions almost 0.25 δ distant from the nearest strip conductor edges where δ is the cell width (See Fig. 1). This method assures high accuracy calculation of characteristic impedance of MSL. To make this arrangement meaningful, magnetic field calculation in a cell having a conductor part in it is done taking conductor-part side lengths into consideration (See Fig. 2).
E. Absorbing Boundary conditions

Generally, we can perform very accurate calculation if Berenger’s PML [8]-[10] are employed for absorbing boundaries. However, more accurate calculation is possible if we could use CFSPML [11]-[13] absorbing boundaries with appropriate parameter values, although this boundary condition has comparatively many parameters to be chosen and its equations and algorithm are somewhat complex. In this paper, CFSPML logic is employed and to create algorithm of calculating fields in PML regions as efficient as possible is one of the most fully worked-out points.

III. ALGORITHM USING GPU

A. Block Division Scheme

GPU calculation of fields in the inner region can be performed throughout by just a single equation, but there are several other kinds of calculation that require different processes or equations for different regions, such as field calculation in PML regions and near around circuit element strip conductors, addition of excitation fields, calculation of port voltages and currents, and so on. It is important to put these calculations into the GPU device as many as possible, yet without increase of computation time. The key technique is to make field calculation in the different regions treatable by a unified equation. This paper’s choice is to discard the unification of field calculation in the z direction (vertical direction), thus the block division scheme employed here is a two dimensional one in the xy plane (transversal plane).

B. Block Dimensions

Variance on the determination of block dimensions is not so vast. It is restricted by the following factors:

1) Generally, the cuboid calculation domain and mesh division cell widths are roughly given beforehand and so the change of mesh division numbers should be slight.

2) FDTD mesh division numbers must be a multiple of the block dimension.

3) Block dimensions must be a power of two.

4) The mesh number of the absorbing boundary interface surface touching to the inner region differs dependent upon the difference of directions and field components, either PML layer number (lc) or that plus one (lc+1). To treat all these cases uniformly, the block dimension is better to be chosen as the number larger than lc.

5) The PML number lc is usually larger than 3 or 4 and smaller than about 20.

Taking account of the above, it is concluded that appropriate number of the block dimension is 16 or 32.

C. Preparation of Device Data

Various variables and arrays are used in the coefficients of field calculation equations. If these variable and array data are sent to the device memory beforehand, computation efficiency will go up. The following is the examples of such array data:

- Coefficient arrays for the calculation of electric fields in the whole region. Arrays are not needed for magnetic fields.
- Coefficient arrays for the calculation of all fields in the upper PML regions.
- Similar arrays as above, but the regions are the side PML regions.
- Coefficient arrays for the calculation of magnetic fields on the strip conductor plane and just above and just below that plane.
- Arrays to select the positions of side PML regions.
- Arrays to select those positions on the strip conductor plane where tangential electric field components reside.
- Arrays to select the points of excitation fields being placed.

D. Calculation steps in GPU Device

With grid and block dimensions given, the calculation steps in the kernel subroutines working in the GPU device are summarized in Fig. 3. As each time step renewed, (a) and (b)

![Fig. 2 Cell with conductor part.](image)

![Fig. 3. Calculation steps in the GPU device. (a) E fields. (b) H fields.](image)
loops are repeated. After each field calculation step finishes, each kernel subroutine exits every time from the device.

E. Field Calculation in PML regions

Explanation is made here using a z=constant cross section located lower than the lowest position of the upper PML region. Figure 4 shows an example of PML regions and block division scheme in such a cross section. Thick lines show the block division lines and thin lines indicate PML region’s boundary planes facing the internal region. The figure is the example of grid dimension of 8 × 6. The notation of PGI fortran is used for block numbers. The regions ② and ③ are side PML regions. In ② and ③, only fields traveling in the y and x directions, respectively, attenuate, while in edge PML regions ④, field attenuation occurs in both directions. To calculate the fields in ② and ③, those of the last time step are needed, and in ④, those of the time step before last are also needed. Thus, to calculate the fields in these PML regions in a single time step, additional calculation of the following four fields is necessary, for which needed are extra array memories corresponding to the fields in the past time steps:

1) Fields corresponding to the y-direction decay time step in ②.
2) Fields corresponding to the x-direction decay time step in ③.
3) Fields corresponding to the y-direction decay time step in ④.
4) Fields corresponding to the x-direction decay time step in ④.

Instead, in the present algorithm, the following highly efficient steps, two steps in effect, are employed:

1) Calculate fields corresponding to the y-direction decay time step in ② and ④.
2) Make new data arrays for ③ + ④ by combining the resultant fields obtained in 1) and the field data of the corresponding positions in ③.
3) Calculate fields corresponding to the x-direction decay time step in ③ + ④.

In the upper side PML regions, z direction decay occurs additionally. Therefore, to calculate the fields in these regions, those corresponding to the z decay time step must be first calculated and then the steps similar to the above steps must be invoked.

IV. Numerical Example

A. Structure of the Example

The step impedance lowpass filter with strip conductor shape as shown in Fig. 5 is taken as a numerical example. The terms “Input” and “Output” in Fig. 5 indicate the positions of input port and output port, respectively, and “Oscillation” means the excitation position. Thickness and relative permittivity of the substrate are 0.787 mm and 2.5, respectively. The expected characteristic impedance of MSL where input or output ports are put is 50 Ω and the cutoff frequency of this filter is expected to be 2.5 GHz.

B. FDTD Parameters

Parameters with respect to FDTD analysis are chosen as follows:

- Three dimensional mesh division: 288 × 192 × 48 (Straight MSL)
  320 × 224 × 48 (Filter structure)
- Cell widths:
  \( \delta x = \delta y = 0.2127214 \ mm \)
  \( \delta z = 0.0787000 \ mm \)
- Substrate thickness division number: 10
- PML layer number: 8 (same in all directions)
- Time increment: \( \delta t = 0.2279 \ ps \)
- Time step number: 4,096 (Straight MSL)
  16,384 (Filter structure)

Cell widths \( \delta x \) and \( \delta y \) correspond to about \( \lambda / 390 \) and \( \delta z \) about \( \lambda / 1,050 \) where \( \lambda \) is the effective wavelength of MSL with a port. Computation is done entirely by single precision.

C. Speedup Rate

Computation time is examined using tesla 2075 as GPU and two Intel Xeon(R) E5620 (each with 4 cores) as processors. OS is Windows 7 Professional and compiler is PGI fortran. Computation is performed for the straight MSL and the step impedance lowpass filter with the parameter values shown above. For the straight MSL, the characteristic impedance is
computed using mode voltage and mode current formed after the pulsed wave propagation of about two wavelengths. For the step impedance filter, the S parameters are calculated using port voltages and currents and characteristic impedance of the corresponding MSL. The acceleration rate when compared to GPU-less calculation is tabulated in Table I. Here, the results using block dimensions of 32 and 16 in the x and y directions, respectively, are shown. Cases (2) and (3) include the calculation of field distributions in a transversal plane in three time steps, while Case (1) does not. Case (3) uses, in this field distribution calculation, algorithm simpler than that of Case (2), and furthermore in Case (3) this calculation is done within GPU device. This is the reason why the acceleration rate of Case (3) is higher than that of Case (2). Acceleration rate for Case (3) is higher than 11 times, even if several data of field distributions in a plane are additionally obtained.

V. CONCLUSION

FDTD solvers for obtaining MMIC passive element circuit characteristics necessarily involve various complex computation processes other than basic FDTD equations. Therefore, it is not so easy to get GPU accelerated good algorithm. By thinking out several new steps of algorithm, this paper attains acceleration rate more than a factor of ten. The author believes that not a few methods shown here are very useful to similar GPU acceleration problems, particularly those on electromagnetic simulation problems.

References