THREE-CONDUCTOR MODELING OF STRIPLINES AT VIA DISCONTINUITIES

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Abstract: In this paper, a model for vias is presented, based on a recently developed stripline model. The via model has been validated based on measurements and field simulations. The influence of inhomogeneous media in the modeling of striplines has been investigated. This via model together with a generic 3-terminal driver model can be immediately implemented in SPICE simulators, much easier than existing via models, such that various factors affecting the return path discontinuity (RPD) caused by vias can be analyzed conveniently.

Key words: return path discontinuity, stripline model, via modeling, non-ideal power distribution, 3-terminal driver model

1. Introduction

Vias that connect signal lines referenced to different planes cause return path discontinuities (RPD), such that the signal return current has to jump between the planes to close the current loop. This in turn excites the parallel-plate mode causing significant electromagnetic emission (EMI) and noise voltage coupling to other vias. If the reference planes are at the same voltage level, then they can be connected with interplane vias at several points near the via transition, to make a low impedance path between the planes. If the planes are at different voltage levels, then decoupling capacitors can be connected at these points.

In [1] a via model was demonstrated for microstrip lines. This paper is an extension of [1] for striplines, using the stripline model of [2]. A parallel-plate transmission line model is used for the planes in this paper. For electrically wide planes, this can be replaced with a 2-dimensional LC network [3] or an interface to an FDTD code [4] to model mode conversion at vias. A major advantage of the stripline model used here is that it is not restricted to vias, such that it can represent mode conversion at any kind of discontinuities (e.g., slots in the reference planes, terminations, etc.). This is a similar approach as in [5], where the signal line is defined as the reference conductor. The stripline model in this paper uses one of the planes as the reference conductor, resulting in fewer elements. It must be noted that these modeling approaches are only valid for striplines in a homogenous medium. In this paper, the influence of inhomogeneous media in the modeling of striplines will also be discussed.

2. Three-Conductor Model

In order to capture the power supply noise and the correct behavior of the return currents, driver and interconnect models that incorporate the signal, power, and ground lines are necessary. In this paper, models which do not assume an ideal power distribution are in general called 3-conductor models. Signal vias in packages having separate planes for the power and ground, can be analyzed using 3-conductor models.

![Figure 1](image-url)

Figure 1 Three-conductor model (top) vs. two-conductor model (bottom)

The 3-conductor model is shown in Figure 1. In this model, the load is represented by capacitors (Cvdd,
Cvss) connected to power (Vdd) and ground (Vss), and the power supply is on the right side of the figure represented by a voltage source (Vsup) and parasitic inductances (Lpow, Lgnd). An arbitrary model is assumed to be available for the interconnect between the driver and the load. If the on-chip and off-chip decoupling capacitors on the driver and load side (Con-dec, Coff-dec) provide infinite decoupling, the power line can be seen as an AC ground. Under this assumption, an equivalent 2-conductor model can be obtained by parallel connecting the power and ground lines as shown in Figure 1. With SI simulations, the interconnect network will be reduced even further to asymmetric π- or T-networks. Via discontinuities, particularly, are commonly represented by π-models consisting of parallel capacitors and a series inductor. The 2-conductor model is not applicable, if there is insufficient decoupling, or if there are many drivers switching simultaneously, such that the power distribution system cannot be regarded as ideal.

![Figure 1](image1)

**Figure 1** Power line model with decoupling capacitors

A simple 3-terminal output driver model has been created as shown in Figure 2, which can be simulated in SPICE. The transistors forming the CMOS driver circuit are modeled using resistors (R1, R2) representing the on-resistance of the devices and voltage controlled switches (S1, S2) with smooth characteristics. The fall and rise times and the period of the inner circuitry driving the CMOS is applied in the simulation through independent voltage sources (V1, V2) connected to these switches. The parasitic capacitance associated with the driver, mainly due to the protection diodes, is represented by two capacitors (C1, C2). Some parallel-connected resistors (R3, R4) with negligible admittance may represent leakage or DC currents and allow that SPICE can make a DC bias point analysis.

![Figure 2](image2)

**Figure 2** Three-terminal driver model for SI and EMC analysis

A single stripline structure between a Vdd and a Vss plane can be considered as a 3-conductor transmission line. For perfect conductors in homogenous media, the modal transformation matrices may not be unique. Intuitively, one of the choices could be the modal decomposition into the parallel plate and the stripline modes. In the parallel plate mode, all of the current flowing into one of the planes returns to the other plane, whereas in the stripline mode, which is the intended mode of operation for signal transmission, there is no voltage difference between the planes. Assume that the Vss plane is chosen as the reference conductor. Based on the definitions of these modes, the transformation matrices can be found under the condition that they must diagonalize the inductance matrix. Accordingly, an equivalent circuit model can be obtained for a stripline as shown in Figure 3. The coupling coefficient is given by

$$k = -\frac{h_1}{h_1 + h_2}, \quad (1)$$

where $h_1$ and $h_2$ represent the distance from the signal line to the Vss and Vdd planes, respectively.

![Figure 3](image3)

**Figure 3** Equivalent circuit model for a stripline in a homogenous medium

The capacitance matrix is automatically diagonalized if the medium is homogeneous. On the other hand, an inhomogeneous medium may not support pure parallel-plate and stripline modes. A capacitive coupling term between the modes has to be considered in this case.

In order to investigate the influence of this capacitive coupling, a test structure composed of substrates with various dielectric constants, as shown in Figure 4, was simulated with Ansoft 2D Extractor.

![Figure 4](image4)

**Figure 4** Test structure to investigate capacitive coupling between the modes

Figure 5 shows the ratio of the off-diagonal term ($C_{12}$) in the mode capacitance matrix to the self-capacitance ($C_{22}$) of the stripline mode. It can be seen that, this ratio can be higher than 15% for some of the configurations considered and grows as the...
dielectric constants of the two substrates diverges. Therefore, this coupling term has to be considered, especially if the difference between the dielectric constants is large.

Figure 5 Ratio of the capacitive coupling term to the capacitance of the stripline mode

4. Modeling of Vias

In Figure 6, the side view of a microstrip to stripline via-transition in a 4-layered package or board can be seen. The signal current returns through the path of least impedance, which is the Vss plane for a trace on the top layer. On the other hand, the return current for the stripline is distributed among the Vdd and Vss planes. A RPD occurs around the via hole, such that a parallel-plate mode is excited. Consequently, noise is injected into the power distribution system (PDS), or conversely, noise on the PDS is coupled to the signal being transmitted.

At high frequencies, the field between the planes and the field surrounding the µ-strip line are uncoupled due to the skin effect. Considering this, the µ-strip can be modeled as a 4-port transmission line using uncoupled µ-strip and parallel-plate transmission line models.

Figure 6 Current paths at a via transition

Since the µ-strip and the stripline are modeled as 4-port structures, they can simply be connected to each other at the via discontinuity, such that the mode-conversions among the µ-strip, stripline, and parallel plate modes are taken into account. Similar to a 2-conductor model, the excessive parasitic elements of the via discontinuity can be represented by a π-model, resulting in a via model as shown in Figure 7. Note that this model depends on a stripline model that assumes a homogeneous medium between the planes. For substrates with different dielectric constants, the capacitive coupling between the stripline and parallel-plate modes must be taken into account. In addition, for electrically wide planes, the parallel-plate transmission line model could be replaced with a 2-dimensional plane model that considers the distributed nature of the plane in both width and length directions.

Figure 7 Three-conductor via model for microstrip to stripline (in a homogeneous medium) transition

5. Experimental Validation

By using the via model in Figure 7, the interconnects of a 4-layered test structure as shown in Figure 8 will be characterized. Only the transmission lines and the planes are considered, so the driver and the power supply shown in the figure are not connected. The lengths of the interconnect segments are $l_1 = l_3 = 5.5$ mm and $l_2 = 6$ mm. The exact widths of the µ-strip, stripline, and the plane pair were obtained from cross-sectional cuts of the structures as 157 µm, 38 µm, and 4 mm, respectively. The top substrate between the µ-strip and the Vss plane, the middle substrate between the Vss plane and the stripline, and the bottom substrate between the stripline and Vdd layer were measured as 120 µm, 141 µm, and 110µm, respectively. Considering that the copper thickness of the stripline is 30 µm, the coupling coefficient in equation (1) can be roughly found as $k=-0.5$. All substrates have a dielectric constant of 4.0 and a loss tangent of 0.025.

Figure 8 Interconnects in a multi-reference plane package

Vss plane is chosen as the reference for the definition of ports. Figure 9 shows the S-parameters representing the coupling between the µ-strip and the Vdd plane at the near end, which is due to the RPD at vias. To obtain the via model, the characteristic impedances of the transmission lines were calculated using Ansoft 2D Extractor. The characteristic impedance of the parallel-plate transmission line was calculated analytically. The excessive via inductance and capacitance were neglected in the model. A very good correlation between measurement and model can be observed.
6. Analysis of Vias

In this section, the influence of vias on the power distribution system will be investigated based on the configuration of Figure 8. To pronounce the influence of vias, all the lengths of the transmission lines are multiplied by 5. The driver and the vias are modeled as shown in Figure 2 and Figure 7, respectively. The transmission lines are assumed to be lossless.

7. Conclusion

A recently developed stripline model is used to investigate the RPD at vias. It is shown that, inhomogeneous media requires special attention in the modeling of the stripline. With this via model, the current return paths and the interaction between the signal transmission and power distribution system can be considered in a simple way by integrating it in a 3-conductor model.

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