A Study on Kv and FTR Trade-off for 28-GHz Band VCO with Variable Inductor Using Switched Resistor

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Abstract This paper presents two configurations of VCOs incorporated a switched resistor for variable inductor, a switched capacitor, and a varactor. The proposed VCOs using a switched resistor contribute to reduce circuit area compared to the VCOs using only a switched capacitor to obtain a narrow frequency step. One configuration was designed for low K_V and the other was for a wide FTR. The simulation results showed the phase noise at 1 MHz offset from 28 GHz carrier frequency of the low-K_V configuration was -100.8 to -101.8 dBc/Hz and that was approximately 0.4 to 0.9 dBc/Hz lower than that of the wide FTR configuration. The oscillation frequency of the wide-FTR configuration was 27.5 to 29.7 GHz, approximately 1.1 GHz wider than that of the low-K_V configuration. The measurement results showed the oscillation frequency was 25.5 to 26.7 GHz and the phase noise was -102.9 to -111.1 dBc/Hz of the wide-FTR configuration. The current consumption was 9.5 to 10.1 mA for the low-K_V configuration and 8.6 to 13.1 mA for the wide-FTR configuration. The process technology used in this study was 180 nm CMOS.

Keyword CMOS, voltage-controlled oscillator (VCO), switched resistor, switched capacitor

1. INTRODUCTION

In recent years, wireless communication technologies such as cellular phones have been progressing dramatically, and the trend towards high frequency to achieve high data rates. For voltage-controlled oscillators (VCO), a wide frequency tuning range (FTR) is required to support various carrier frequencies for cellular phones even at high frequencies. The way to extend the FTR of VCO, the combination of switched capacitor and varactor is frequently used, where a switched capacitor is used for coarse tuning and a varactor is used for fine tuning. However, since the noise in the circuit is converted to frequency fluctuation by the VCO gain (K_V), a VCO with low K_V is required to achieve low phase noise.

In our laboratory, LC oscillators that fine-tune the frequency without using a varactor have been studied as a method independent of K_V[1,2]. In ref. 1, it was studied a digital-controlled oscillator (DCO) with a switched inductor by switching 14-bit MOS-SW which was independent of K_V, and the DCO performed at 12.4 to 12.6 GHz (FTR = 1.6%). Also in ref. 2, a DCO with a switched resistor was studied by switching 13-bit MOS-SW which was independent of K_V, and the DCO performed at 27.2 to 27.6 GHz (FTR = 1.9%). Therefore, our previous research found that achieving a wide FTR is difficult in a situation independent of K_V.

From this background, it is considered to be a trade-off relationship between K_V and FTR. Therefore, in this study, as a new method to reduce K_V while achieving a wide FTR, this paper presents two configurations of VCOs that operate at 28 GHz-band with a switched inductance by a switched resistor in addition to a switched capacitor and varactor. One configuration was designed for low K_V and the other was designed for a wide FTR.

2. CIRCUIT DESIGN

In this study, an inductor of the transformer structure was equipped with the proposed circuits to obtain a narrow frequency step by the inductance switched by switching the resistors with MOS-SW that connected to the secondary side of the transformer. Such a narrow frequency step can be realized by switching the capacitors, however, it needs tiny capacitance steps. Since the limitation of capacitor size due to design rule constraints, capacitors have to connect series to realize small capacitance, result, the occupied area of the frequency switching part will be huge. Specifically, in the VCO circuit of a wide-FTR configuration in this study, the frequency has to be varied by about 300 MHz by controlling with a fine switching. To realize it, when controlling for the frequency range with switched capacitors, 4 fF of capacitance is required and that means five pieces of

9.2×15.2 μm2 (≈20 fF) capacitors, the minimum size of the capacitor of the process used in this study, must be connected in series. On the other hand, when controlling for the frequency range with a switched inductor by the switches resistors, 315 Ω and 473 Ω resistances are required and that means only 10 pieces of 1.2 × 3.0 μm2 (≈946 Ω) are connected in parallel. This is thought to reduce the area of the circuit of this portion by about 1/20 compared to the case of using a switched capacitor.

2.1. CIRCUIT CONFIGURATIONS

Figure 1 shows the proposed circuits of two configurations of VCOs. The first configuration was aimed for low K_V by applying a narrow range of voltages to the varactor, and the second one was aimed for a wide FTR by applying a wide range of voltages to the varactor. Figure 2 shows the structure of the secondary side of both circuits. Each circuit has the same structure of the primary side of the transformer, but the secondary side is different. The secondary side of the first configuration circuit consists of a 3-bit switched capacitor and a 3-bit switched resistor. On the other hand, the second configuration consists of a 3-bit switched capacitor and a 2-bit switched resistor. The switched capacitor and switched resistor are controlled with MOS-SW, respectively. The total capacitance of the circuit is changed by the switched capacitor for frequency course-tuning and the total inductance of the transformer is changed by the switched resistor for frequency fine-tuning.

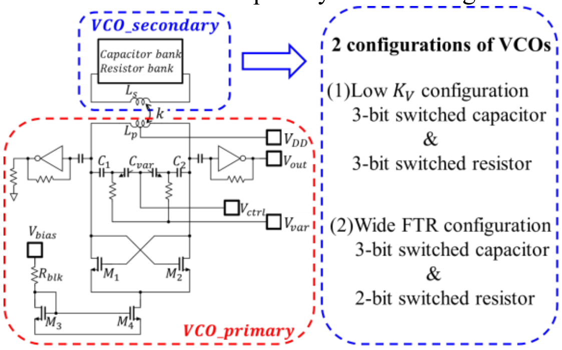

Fig. 1 Proposed circuit of two configurations of VCOs.

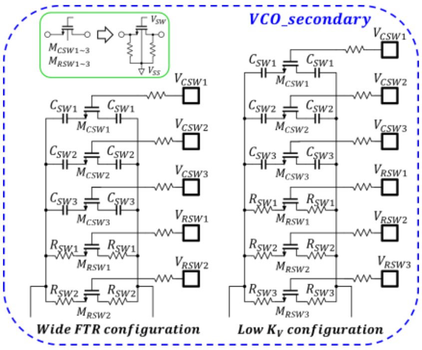

Fig. 2 The structure of the secondary side of two configurations of VCOs.

2.2. VARIABLE INDUCTANCE WITH THE SWITCHED RESISTOR

Figure 3 shows the equivalent circuit of the part of the transformer of the circuit as shown in Fig. 1. The voltage of the primary side is v_p and the secondary side is v_s. Each voltage is represented by Eq. (1) – (2), where, R_{Lp} is the parasitic resistance on the primary side, R_{SW} is the total resistance on the secondary side, L_p is the inductance on the primary side, L_s is the that on the secondary side, i_p is the current on the primary side, i_s is the that on the secondary side, $M = k\sqrt{L_pL_s}$, and k is coupling coefficient between L_p and L_s. The current on the secondary side is calculated by Eq. (1) – (2), which is shown in Eq. (3).

$$v_p = \left(R_{L_p} + j\omega L_p\right) i_p \pm j\omega M i_s \tag{1}$$

$$v_s = (R_{SW} + j\omega L_s) i_s \pm j\omega M i_p \tag{2}$$

$$i_s = -\frac{j\omega M}{R_{SW} + j\omega L_s} i_p \tag{3}$$

Substituting Eq. (3) into Eq. (1), Eq. (4) is calculated and Eq. (5) is obtained by dividing both sides by i_p, which means the total impedance on the primary side, Z_p. Therefore, from Eq. (5), the total inductance on the primary side is represented by Eq. (6). From Eq. (6), the total inductance, L_{tot}, can be controlled by carrying the resistance of the secondary side.

$$v_p = \left(R_{L_p} + j\omega L_p\right) i_p + \frac{R_{SW}(\omega M)^2}{R_{SW} + j\omega L_s} i_p \tag{4}$$

$$\frac{v_p}{i_p} = Z_p$$
$$= R_{L_p} + \frac{R_{SW}\omega^2 k^2 L_s L_p}{R_{SW}^2 + (\omega L_s)^2} + j\left(\omega L_p - \frac{\omega^3 k^2 L_s^2 L_p}{R_{SW}^2 + (\omega L_s)^2}\right) \tag{5}$$

$$L_{tot} = L_p\left(1 - \frac{(k\omega L_s)^2}{R_{SW}^2 + (\omega L_s)^2}\right) \tag{6}$$

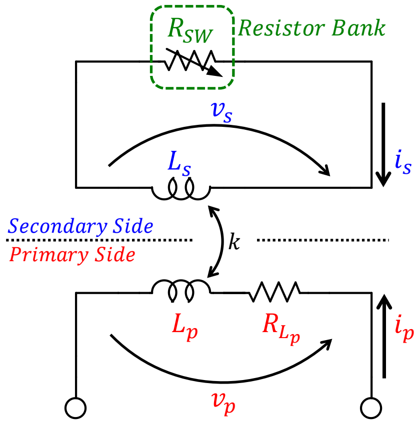

Fig. 3 Equivalent circuit of the transformer and its peripheral.

2.3. INDUCTOR STRUCTURE

Figure 4 shows the bird's-eye view of the inductor of the transformer structure used in this study. This structure is modified of the inductor which has been studied in our laboratory[3]. Table 1 shows the parameters of the inductor of the two configurations of the VCOs. The inner radius of the inductor for the low-K_V configuration is 39 µm, and that for the wide-FTR configuration is 37 µm. About the low-K_V configuration, the inductance on the primary side is 168 pH and the secondary side is 166 pH at 28 GHz, the Q-factor on the primary side is 16.1 and the secondary side is 9.6 at 28 GHz, the coupling coefficient is 0.89 at 28 GHz of the inductor. While, about the wide-FTR configuration, the inductance on the primary side is 155 pH and the secondary side is 157 pH at 28 GHz, the Q-factor on the primary side is 16.6 and the secondary side is 9.0 at 28 GHz, the coupling coefficient is 0.89 at 28 GHz of the inductor.

Both inductors have the same structure which has metal 6 shorted to metal 4 in the out of the inductor winding, and metal 5 shorted to metal 3 in the out of the inductor winding. The coupled inductor consisting of metal 6 and metal 4 is connected to the primary side of VCO, and the inductor consisting of metal 5 and metal 3 is connected to the secondary side of VCO. Because of the structure of the vertically coupled inductor, it has a high coupling coefficient and to control the resistance on the secondary side of VCO is expected to contribute to variable inductance through mutual induction.

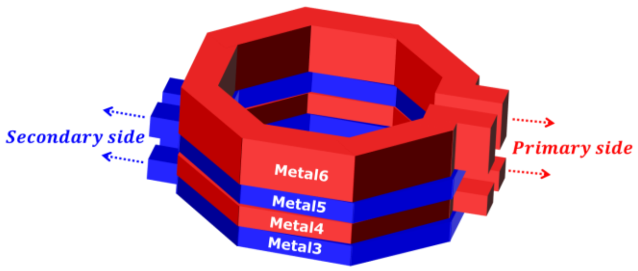

Fig. 4 Bird's-eye view of the inductor of the transformer structure.

Table 1 Parameters of two configurations of the inductors at 28 GHz

Configuration	*Radius* [um]		*L* [pH]	*Q*	*k*
For low K_V	39	L_p	168	16.1	0.89
		L_s	166	9.6	
For wide FTR	37	L_p	155	16.6	0.89
		L_s	157	9.0	

2.4. SWITCHED CAPACITOR AND SWITCHED RESISTOR

Figure 5 shows the equivalent circuit of the switched capacitor and switched resistor on the secondary side of the two configurations of VCOs. For low-K_V configuration, the secondary side consists of a 3-bit switched capacitor of coarse-tuning and a 3-bit switched resistor of fine-tuning. For a wide-FTR configuration, the secondary side consists of a 3-bit switched capacitor of coarse-tuning and a 2-bit switched resistor of fine-tuning. Each switched capacitor and switched resistor is switched by using MOS-SW.

Table 2 shows the parameters of two configurations of VCOs. For low-K_V configuration, the gate W/L of $M_{CSW1\sim3}$ is 12 µm/180 nm, and that of $M_{RSW1\sim3}$ is 54 µm/180 nm. The coarse-tuning capacitor bank is controlled by 3-bit MOS-SWs, thus $2^3=8$ different capacitance values are obtained, and the fine-tuning resistor bank is controlled by 3-bit MOS-SWs, thus $2^3=8$ different resistance values obtained, in addition, as a bit-to-bit adjustment of the 3-bit switched resistor, a control voltage of 0.5 to 1.0 V is applied to the varactor. While, for a wide-FTR configuration, the gate W/L of $M_{CSW1\sim3}$ is 12 µm/180 nm, and that of $M_{RSW1\sim3}$ is 21 µm/180 nm. The coarse-tuning capacitor bank is controlled by 3-bit MOS-SWs, thus $2^3=8$ different capacitance values are obtained, and the fine-tuning resistor bank is controlled by 2-bit MOS-SWs, thus $2^2=4$ different resistance values obtained, in addition, as a bit-to-bit adjustment of the 2-bit switched resistor, a control voltage of 0.6 to 1.5 V is applied to the varactor. The oscillation frequency is represented as shown in Eq. (7), where, f_{osc} is the oscillation frequency, L_{tot} is the total inductance seen from the primary side as shown in Eq. (6), C_{SW} is the total capacitance of the switched capacitor on the secondary side, C_{var} is the capacitance of the varactor, and C_P is the parasitic capacitance.

$$f_{osc}=\frac{1}{2\pi\sqrt{L_{tot}(C_{SW}+C_{var}+C_P)}} \tag{7}$$

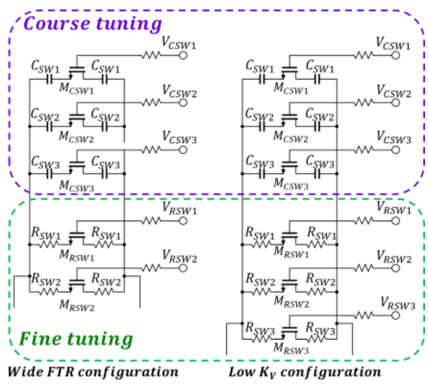

Fig. 5 Equivalent circuit of the secondary side of two configurations of VCOs.

Table 2 Parameters of two configurations of VCOs

Configuration	*Low K_V configuration*	*Wide FTR configuration*
V_{DD}, V_{var} [V]	1.8, 0.9	1.8, 0.9
V_{ctrl} [V]	0.5~1.0	0.6~1.5
I_{DD} [mA]	9.5~10.4	8.6~13.1
$C_{SW1\sim3}$ [fF]	34.9, 21.4, 13.7	60.4, 35.0, 21.0
$R_{SW1\sim3}$ [Ω]	345.7, 518.6, 1037.3	315.3, 473.0
$M_{CSW1\sim3}$	12 μm/180 nm	12 μm/180 nm
$M_{RSW1\sim3}$	54 μm/180 nm	21 μm/180 nm

3. SIMULATION RESULTS

The parameter values of the circuit in Fig. 1 were set as Table 2 and simulations were performed. Considering the frequency variation during chip manufacturing, the current in the circuit was optimized so that the frequency overlapped by 10 to 20 MHz for each state of the switched capacitor.

Figures 6 and 7 show the simulation results of the oscillation frequency dependence of the K_V. Each color represents the state of the switched capacitor and each line represents the state of the switched resistor. Figure 6 shows that the simulation result of the oscillation frequency was 27.80 to 28.93 GHz, the FTR was 3.97%, and the K_V was 37 to 109 MHz/V. with a power consumption of 9.5 to 10.4 mA. Figure 7 shows that the simulation result of the oscillation frequency was 27.50 to 29.74 GHz, the FTR was 7.84%, and the K_V was 46 to 141 MHz/V with a power consumption of 8.6 to 13.1 mA. From the simulation result, the frequency range of the wide-FTR configuration was approximately 1.1 GHz wider than that of the low-K_V configuration, while, the K_V of the low- K_V configuration was approximately 11 to 32 MHz/V lower than that of the wide-FTR configuration.

Figures 8 and 9 show the simulation results of the oscillation frequency dependence of the phase noise at 1 MHz offset from the 28 GHz carrier frequency. Each color represents the state of the switched capacitor and each symbol represents the state of the switched resistor. Figure 8 shows that the simulation result of the phase noise was −100.8 to −101.8 dBc/Hz. Figure 9 shows that the simulation result of the phase noise was −99.9 to −101.4 dBc/Hz. From the simulation result, the phase noise of the low-K_V configuration was approximately 0.4 to 0.9 dBc/Hz lower than that of the wide-FTR configuration.

Figure 10 shows the simulation results of the average K_V comparison of two configurations of VCOs. The color red represents the low- K_V configuration and the color blue represents the wide-FTR configuration. Each line represents the state of the switched capacitor and the horizontal axis of the graph represents the state of switched resistor. Figure 10 shows that the simulation result of the average K_V of the low-K_V configuration was 66.3 to 75.1 MHz/V, and that of the wide-FTR configuration was 87.2 to 114 MHz/V. From the simulation result, the average K_V of the low-K_V configuration was approximately 21 to 39 MHz/V lower than that of the wide-FTR configuration.

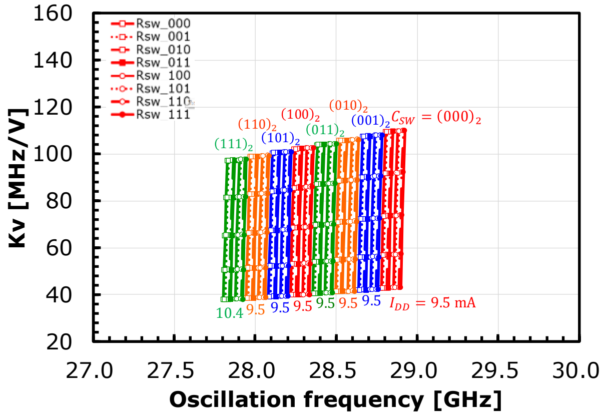

Fig. 6 Simulation results of the oscillation frequency dependence on the K_V(Low-K_v configuration).

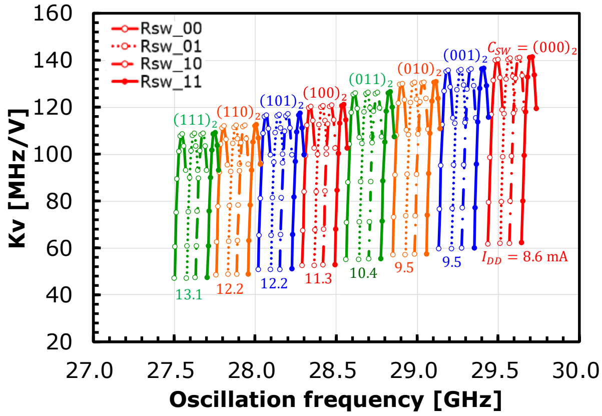

Fig. 7 Simulation results of the oscillation frequency dependence on the K_V(Wide-FTR configuration).

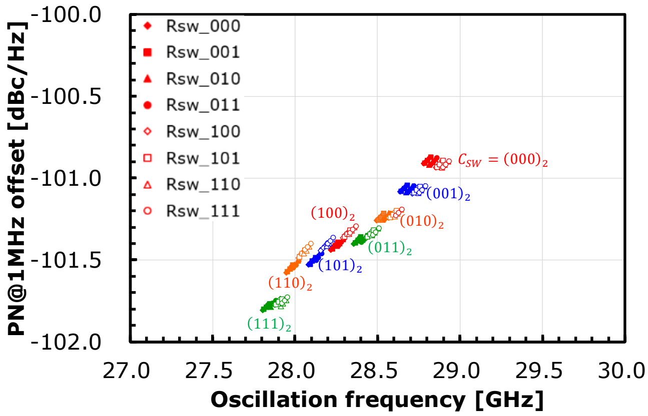

Fig. 8 Simulation results of the oscillation frequency dependence on the phase noise(Low-K_v configuration).

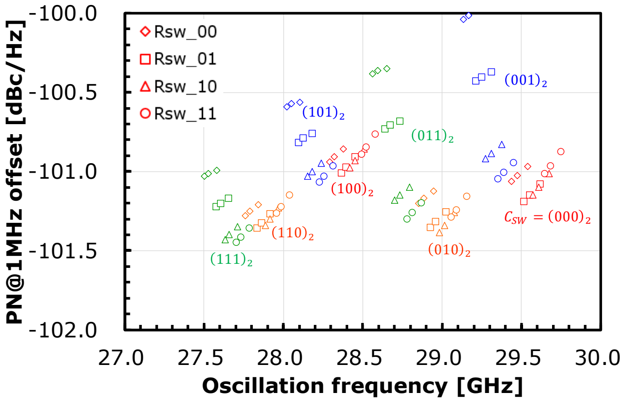

Fig. 9 Simulation results of the oscillation frequency dependence on the phase noise (Wide-FTR configuration).

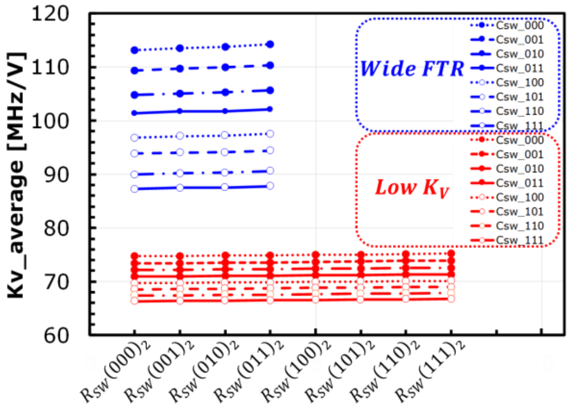

Fig. 10 Simulation results of the average K_V comparison of two configurations of VCOs.

4. MEASUREMENT RESULTS

Since we have not obtained adequate measurement data yet, this chapter presents a portion of the measurement results of the wide-FTR configuration.

Figure 11 shows the chip photo of two configurations of VCOs. The circuit area of the wide-FTR configuration was 580×630 μm^2 and the circuit area of the low-K_V configuration was 680×630 μm^2.

Figure 12 shows the measurement results of the oscillation frequency dependence on the control voltage of the wide-FTR configuration. Each color represents the state of the switched capacitor and each line represents the state of the switched resistor. According to Fig. 12, the measurement result of the frequency was 25.53 to 26.79 GHz with a control voltage of 0.6 to 1.5 V, the FTR was 4.81% with a current consumption of 8.1 to 12.8 mA.

Figure 13 shows the measurement results of the oscillation frequency dependence on the K_V of the wide-FTR configuration. Each color represents the state of the switched capacitor and each line represents the state of the switched resistor. According to Fig. 13, the measurement result of the K_V was 40 to 100 MHz/V and the average K_V was 63.7 MHz/V.

Figure 14 shows the measurement results of the oscillation frequency dependence on the phase noise at 1 MHz offset from the 28 GHz carrier frequency of the wide-FTR configuration. Each color represents the state of the switched capacitor and each shape represents the state of the switched resistor. According to Fig. 14, the measurement result of the phase noise was −102.9 to −111.1 dBc/Hz.

Performance comparison of measurement and simulation results of VCO are shown in Table 3.

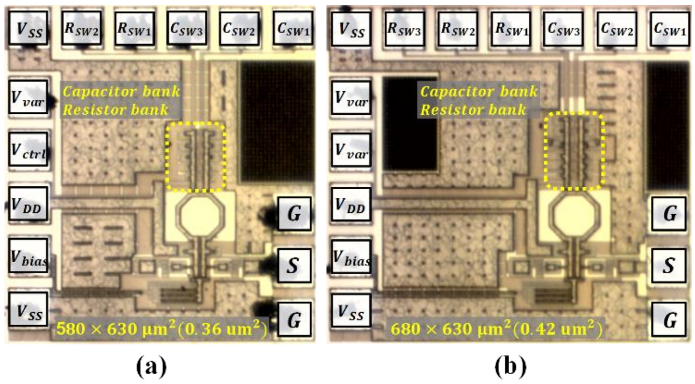

Fig.11 The chip photo of two configurations of VCOs. (a)Wide-FTR configuration, (b)Low-K_V configuration

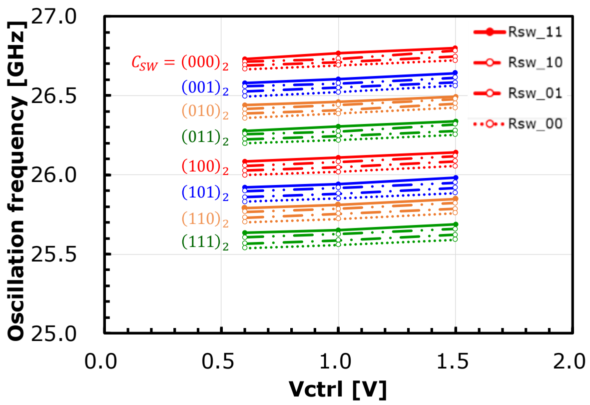

Fig. 12 Measurement results of the oscillation frequency dependence on the control voltage (Wide-FTR configuration).

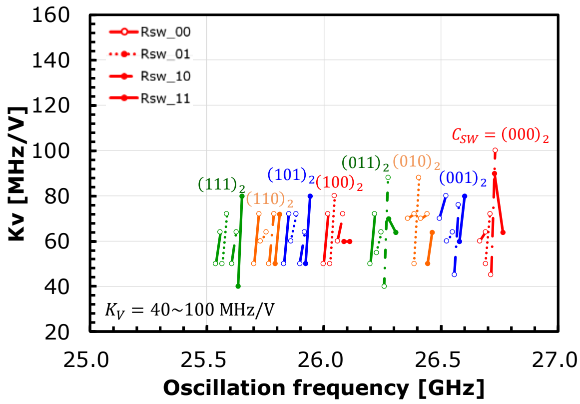

Fig. 13 Measurement results of the oscillation frequency dependence on the K_V(Wide-FTR configuration).

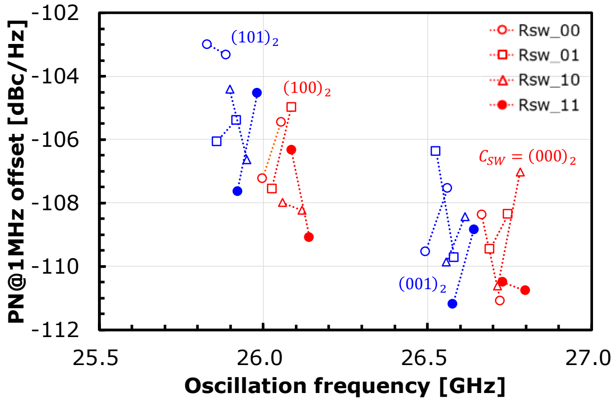

Fig. 14 Measurement results of the oscillation frequency dependence on the phase noise (Wide-FTR configuration).

Table 3 Performance comparison of VCO

Ref.	Process	freq. [GHz]	PN@1MHz [dBc/Hz]	Power Consumption [mA]	Chip Area [mm^2]	Year
[4]	180 nm CMOS	24.5 to 27.25	−102	43.6	0.76	2020
[5]	28 nm CMOS	20.7 to 31.8	−103.6	5.5	0.06	2018
[6]	65 nm CMOS	21.95 to 24.25	−100.7	8.0	0.19	2019
[7]	90 nm CMOS	27.5 to 30.04 55 to 60.08	−95.6 −87.8	7.0	0.41	2021
This Work *Low K_V (sim.)*	180 nm CMOS	27.8 to 28.9	−100.8 to −101.8	9.5 to 10.4	0.42	2023
This Work *Low K_V (meas.)*		*N.A.*	*N.A.*	*N.A.*		
This Work *Wide FTR (sim.)*		27.5 to 29.7	−99.9 to −101.4	8.6 to 13.1	0.36	
This Work *Wide FTR (meas.)*		25.5 to 26.7	−102.9 to −111.1	8.1 to 12.8		

5. CONCLUSION

In this study, two configurations of VCOs with variable inductors using a switched resistor were designed. For the low- K_V configuration, the simulation results of the oscillation frequency was 27.80 to 28.93 GHz, the FTR was 3.97%, the phase noise was −100.8 to −101.8 dBc/Hz, the average K_V was 66.3 to 75.1 MHz/V with the power consumption of 8.6 to 13.1 mA. While, for the wide-FTR configuration, the oscillation frequency was 27.50 to 29.74 GHz, the FTR was 7.84%, the phase noise was −99.9 to −101.4 dBc/Hz, the average K_V was 87.2 to 114 MHz/V with the power consumption of 9.5 to 10.4 mA. The measurement results of the oscillation frequency of wide-FTR configuration was 25.53 to 26.79 GHz, the FTR was 4.81%, the phase noise was −102.9 to −111.1 dBc/Hz, the average K_V was 63.7 MHz/V with a power consumption of 8.1 to 12.8 mA. Comparing both configurations, the FTR of the wide-FTR configuration was superior to that of the low-K_V configuration, however, because of the lower K_V, the phase noise of the low-K_V configuration was superior to that of the wide-FTR configuration.

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