A Micropower CMOS Preamplifier for Cochlear Implant System

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Abstract: This paper proposes a CMOS low-power low-voltage microphone preamplifier for a cochlear implant system. The proposed preamplifier using the Flipped Voltage Follower Current Sensing (FVFCS) technique to achieve low voltage, low power consumption. The proposed circuit was designed and simulated using a 0.35 μm CMOS process. Simulation results showed that the preamplifier can achieve 22-dB voltage gain while dissipating only 5.2 µW from 1.4-V power supply voltage.
Keywords: Cochlear Implant System, Transimpedance Amplifier, Microphone Preamplifier, Low-power CMOS.

1. Introduction

Cochlear Implant (CI) can restore partial hearing to deaf people by stimulating the auditory nerve in response to sound in a manner similar to that of the real human ear [1] - [3]. Fig.1 shows an example of a cochlear implant system. A microphone picks up sound and converts it to an electrical signal, which is processed by a speech signal processor. The processor normally consists of preamplifier, automatic gain control (AGC), bandpass filters, envelope detectors and analog-to-digital converters (ADC). The outputs of ADCs are scanned and sent to the electrodes for nerve stimulation.

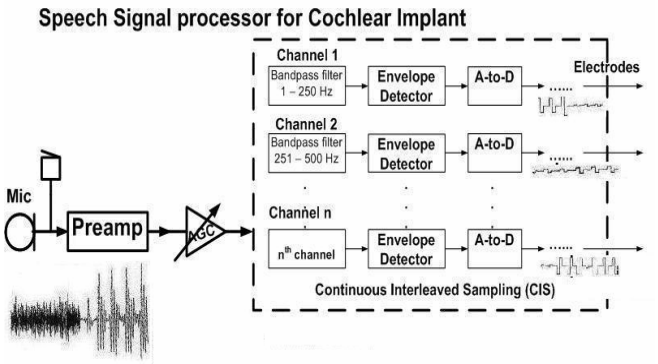


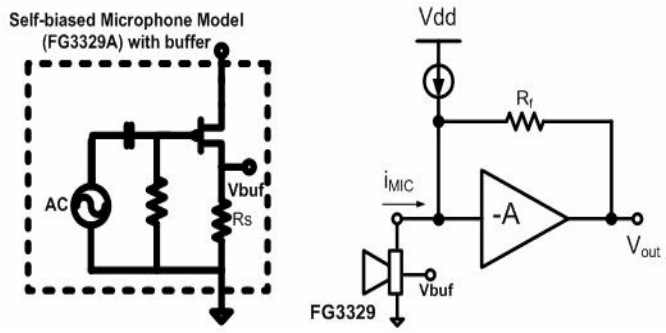
Fig.1. Block diagram of a Cochlear Implant System.

A low-power, wide dynamic range microphone preamplifier with good wide-band rejection of power supply noise is required for CI systems. Traditionally, the buffered voltage output of an electret capacitor with a built-in JFET source follower is used as the input of the preamplifier. Recently, a low-power high-PSRR current-mode preamplifier has been proposed [4], by sensing the JFET microphone buffer current output rather than its voltage output. The circuit in [4] operated with 2.8-V power supply voltage and dissipated 36 µW. This paper aims to propose a simple low-voltage micropower preamplifier based on the same current-sensing strategy as in [4]. The proposed circuit has been designed and simulated by using Cadence Spectre with process parameters a 0.35-µm CMOS technology.

The organization of this paper is as follows. In section 2, we discuss in transimpedance amplifier design base on the FVFCS technique, we shall present possible low voltage transimpedance amplifiers that uses a current mode amplifier. In section 3, we present simulation results. Finally, conclusions are made in section 4.

2. Circuit Description

Fig. 2 shows a simplified diagram of the current-sensing topology proposed in [4]. The supply current of a self-biased JFET microphone, rather than its buffered output voltage, is sensed and used as the input of the preamplifier. The sensed current converted to an output voltage by a transimpedance amplifier, with a gain determined by the feedback resistor R_f. The key advantage of this topology is the voltage regulation of the drain node of JFET which leads to better power supply noise rejection.



(a) (b)

Fig.2 (a) Self-biased Microphone Model with FET buffer. (b) Block diagram of Microphone Preamplifier.

2.1 Transimpedance Amplifier

The transimpedance amplifier is implemented as shown in Fig. 3 [5]. Transimpedance amplifier is realized with a current amplifier with a feedback resistor R_f. The current amplifier is simply realized by using a scaled cascode current mirror, with a mirror ratio of α. The input current

flows into M_2 and is copied to M_3 and the output, with a current gain of α.

With the feedback resistor R_f, the DC transimpedance gain is approximately given by (1), assuming that $R_f >> 1/g_{m3}$.

$$R_m = \frac{v_{out}}{i_{in}} = \frac{\left(\frac{1}{g_{m3}} - R_f\right)}{\left(1+\frac{1}{\alpha}\right)} \approx -\frac{R_f}{\left(1+\frac{1}{\alpha}\right)} \quad (1)$$

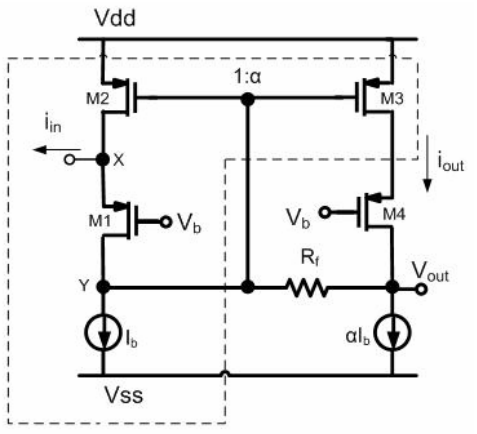


Fig.3 Transimpedance Amplifier.

In the dashed box of Fig.3 is FVFCS technique, base on FVF [6]. The FVF can provide a current sensing cell. The impedance at node X is very low, thus the voltage at the input is nearly constant. Large current can be sourced at the input node. The large sourcing capability is due to the low impedance at the output node.

2.2 Proposed Preamplifier

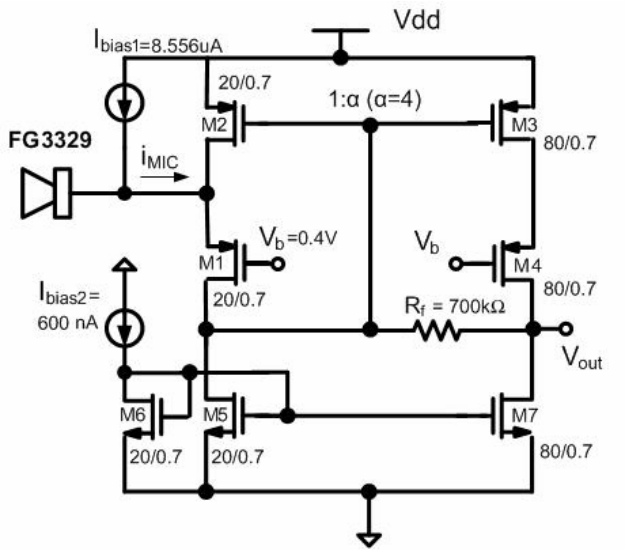


Fig.4 Proposed Preamplifier.

The proposed preamplifier, rather than the conventional two-stage operational amplifier as in [4], can be employed to reduce power supply voltage and power dissipation further. A simple transimpedance amplifier is realized with a current amplifier with a feedback resistor R_f, as shown in Fig. 4 [5].

2.3 Noise Analysis

Considering thermal noise sources only, the input-referred noise of the transimpedance amplifier cell can be calculated as given by (2), where, $\overline{i_{ni}^2} \approx 4kTg_{mi}\Delta f$, $\overline{v_{n,R_f}^2} \approx 4kTR_f\Delta f$, and A_{vo} is the voltage gain. Assuming that $g_{m2}R_f >> 1$ and $g_{m3} = g_{m2}$, the input referred noise is estimated by (3), Thus the input-referred noise can be reduced by increasing g_{m1} and the voltage gain.

$$\overline{v_{ni}^2} = \frac{1}{g_{m1}^2}\left(\overline{i_{n1}^2} + \overline{i_{n2}^2}\right) + \overline{v_{n,R_f}^2}\left|\frac{1}{A_{vo}}\right|^2 + \overline{i_{n3}^2}\left|\frac{1+g_{m1}(1+g_{m2}R_f)}{g_{m1}\left(-1+g_{m3}R_f\right)}\right|^2 \quad (2)$$

$$\overline{v_{ni}^2} \approx \frac{1}{g_{m1}^2}\left(\overline{i_{n1}^2} + \overline{i_{n2}^2}\right) + \overline{i_{n3}^2} + \overline{v_{n,R_f}^2}\left|\frac{1}{A_{vo}}\right|^2 \quad (3)$$

3. Simulation Results

The proposed preamplifier has been designed and simulated with Cadence Spectre with process parameters from a 0.35-μm CMOS technology. The circuit was designed to operate under a 1.4 V power supply voltage. The total power consumption is 17.1 μW, which includes 11.9 μW for the microphone built-in buffer and 5.2 μW for proposed preamplifier. Transistors sizes and bias currents are shown in Fig. 4. Table I summarizes the simulated performance of the proposed circuit. Simulation results in Fig. 5 showed that the circuit could achieve an overall gain of 22 dB, 77-kHz gain-bandwidth product and 74° phase margin with 5-pF load capacitor. Fig. 6 shows the simulated input-referred noise spectral density over 10-kHz bandwidth. The total integrated input-referred noise is

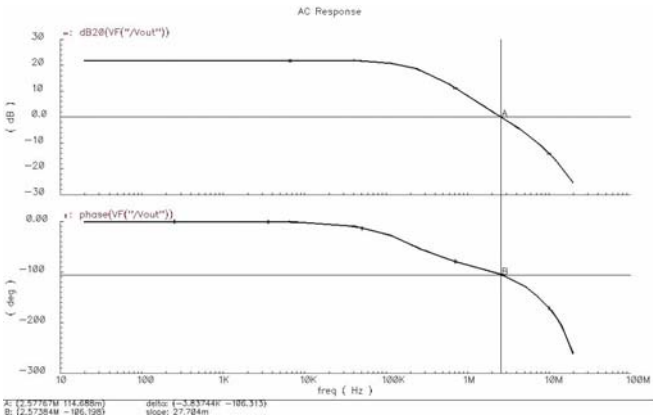


Fig.5. Simulated frequency response of the amplifier.

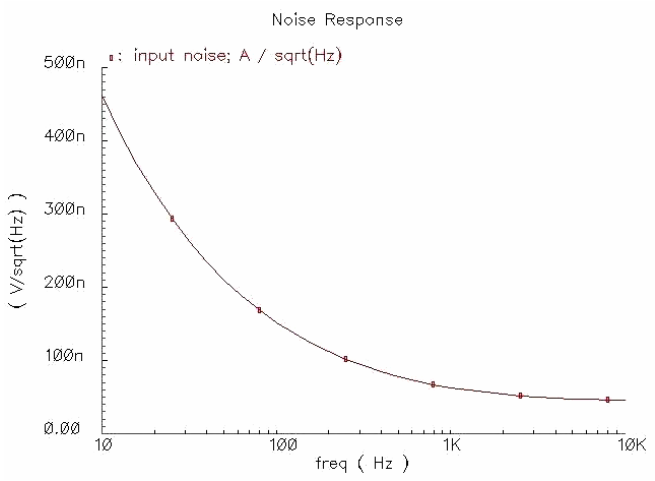
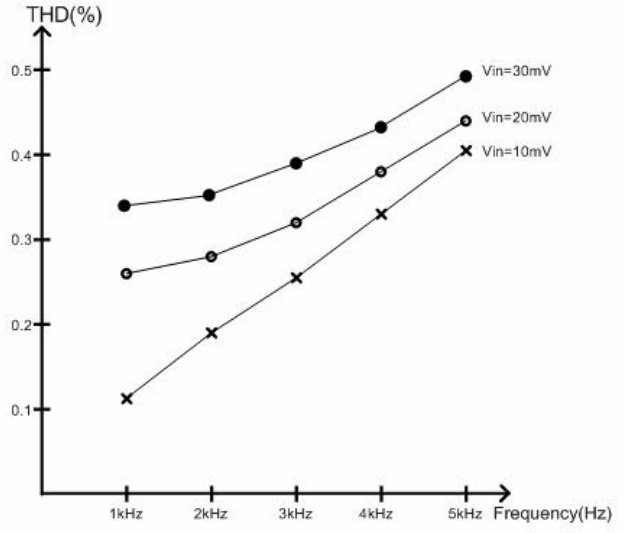
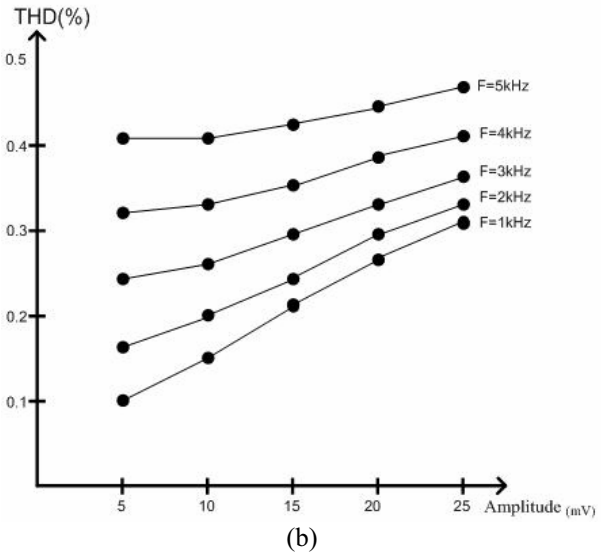


Fig.6. Noise spectral density.



(a)



(b)

Fig.7. Total Harmonic Distortion: THD (%)

Fig. 7 shows the simulated total harmonic distortion (THD) of the amplifier at different input frequencies and amplitudes. It can be seen that the output THD can be kept below 0.5% throughout the expected operating range of input frequencies and amplitudes of the preamplifier.

Table I. Summary of the simulated performance of the proposed amplifier

Parameters	Ref. [4]	Ref. [7]	This work
CMOS Technology	1.5 μm	1.2 μm	0.35 μm
Power Supply	2.8 V	+/-1.5 V	1.4 V
Phase margin	>60 deg	-	74 deg
DC Gain (dB)	20 dB	20 dB	22 dB
Unity-gain frequency (Hz)	-	-	77 kHz
Power consumption	36 µW	24 µW	5.2 µW
Total input-referred noise (10-10kHz)	-	30 µV	5.7 µV

4. Conclusion

This paper describes the design and realisation of a new CMOS microphone preamplifier a cochlear implant system. The proposed circuit employed shunt-feedback and current-sensing topology to achieve low-voltage and low-power operation. Simulation results showed that the preamplifier could achieve competitive performance with previously reported work, while operating with lower power dissipation and supply voltage. The authors believe that the proposed amplifier has a strong potential for biomedical applications.

Acknowledgements

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