ANALYSIS OF I/O CLAMP, POWER CLAMP ESD PROTECTION CIRCUIT

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Abstract: This paper presents a ESD protection device for I/O clamp and power clamp. The proposed ESD protection devices has a fast turn on time, low trigger voltage, and high holding voltage characteristics than conventional ESD protection device. The proposed device was analyzed to figure out electrical characteristics and tolerance robustness in term of individual design parameters (D1, D2, D3). They are investigated by using the Synopsys TCAD simulator. The results show that the STNMOS (Substrate Triggered NMOS) device has lower trigger voltage 4.8V compared to the conventional GGNMOS. In addition the proposed a novel SCR (Silicon Controlled Rectifier) - based ESD (Electrostatic Discharge) protection device for power clamp. The proposed device has a higher holding voltage characteristic than conventional SCR. These characteristics enable to have latch-up immunity under normal operating conditions as well as superior full chip ESD protection. As a result of simulation, holding voltage increased with different design parameters. The holding voltage of the proposed device changes from 3.3V to 7.9V.

1. Introduction

The development of semiconductor process technologies brought about the miniaturization of ICs (Integrated devices), but the failure of device by ESD (Electrostatic Discharge) is becoming a more serious problem. Furthermore, with the increasing demand for analog and high-voltage IC technologies, the ESD protection device is being regarded as important for the reliability of IC [1]. The schematic of whole chip ESD protection circuit are shown in Figure 1. The silicide-blocked GGNMOS (Gate Grounded NMOS) is the common ESD protection structure[2]. Typically, multi-finger GGNMOS devices are widely used as ESD Clamp due to its easy design and perfect compatibility with CMOS process. However, it has been reported that multi-finger GGNMOS can not be uniformly turned on under ESD condition [3-6].

The substrate trigger technique using PMOS is used to reduce the trigger voltage and to achieve turn-on uniformity of multi-finger GGNMOS. Despite of the Substrate trigger technique, STNMOS have low current driving and consumes a relatively larger silicon area. So, For Power-rail ESD clamp, SCR(Silicon Controlled Rectifier) can be great candidate for ESD protection owing to its higher ESD robustness and smaller area than GGNMOS.[7] However, due to low holding voltage, they have still transient-induced latch-up problem[8]. The latch-up problem can be overcome by increasing the holding current or holding voltage. Therefore, in this paper in introduces a STNMOS (Substrate Triggered NMOS) and a SCR based device with high holding voltage, For I/O and power clamp, respectively.

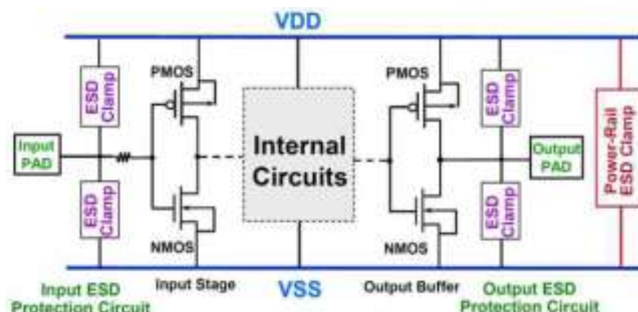
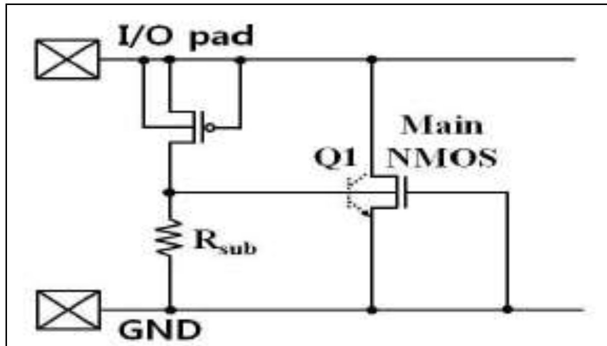


Figure 1. The schematic of whole chip ESD protection circuit

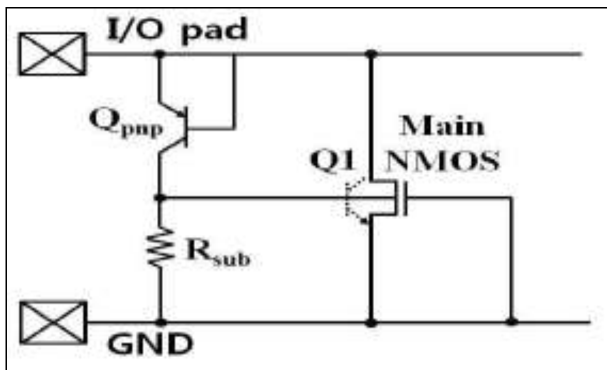
2. OPERATION OF THE ESD PROTECTION

2.1 I/O clamp ESD protection device

The substrate trigger technique is used widely to reduce the trigger voltage and to enhance turn-on uniformly of GGNMOS. Figure 2(a) shows conventional STNMOS (Substrate Triggered NMOS) using PMOS. However, the conventional method has two problems due to the use of PMOS. The first problem is that the trigger PMOS with a long channel length which reduces gate leakage slows turn-on time. The second is that the gate oxide of the trigger PMOS can be easily broken down by ESD surge. These problems are solved by using PNP bipolar transistors instead of trigger PMOS as shown in Figure. 2(b) Two problems mentioned earlier are solved by using PNP bipolar transistors in place of PMOS. The operation of proposed structure is as follows. When a positive ESD voltage is applied on the I/O pad, the PNP bipolar transistors (Qpnp) triggers by avalanche breakdown of the base-collector junction region. Hole current will flow in the base region of the parasitic bipolar transistor (Q1) in the main NMOS. Thus, It contribute to forward bias base-emitter junction of the parasitic bipolar transistor (Q1). As a result, the triggered voltage is reduced, the turn-on uniformity of multi-finger GGNMOS is enhanced.



(a)



(b)

Figure 2. (a) Conventional STNMOS using PMOS. (b) Proposed substrate-triggered NMOS using PNP bipolar transistor

2.2 Power Clamp ESD protection device

Cross section of conventional SCR is shown in Figure.3. When ESD surge is applied to SCR, junction between N-well and P-well is reverse biased. As anode voltage increases, the junction occurs avalanche breakdown. Generated current makes voltage drop and NPN parasitic bipolar transistor turns on. After NPN transistor turns on, its current makes PNP transistor turns on. These NPN/PNP transistors operate in positive feedback and it makes relatively low holding voltage about 2V. This low holding voltage leads to latch-up problem during normal operation condition. Therefore, we propose modified SCR-based ESD devices with high holding voltage.[9]

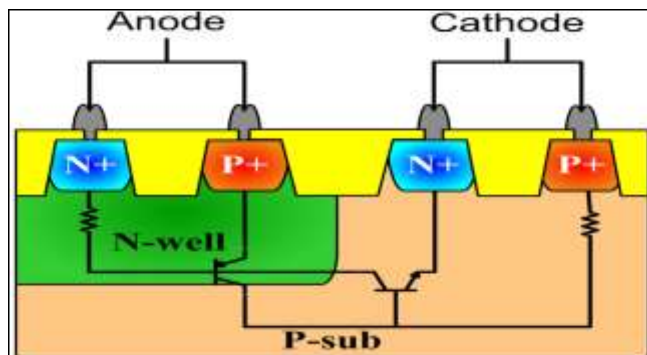


Figure 3. Cross section of conventional SCR ESD protection devices

Proposed SCR-based ESD protection device was transformed and the floating n+ expansion area inserted in n-well area was added. Then, p+ cathode (p-drift) was expanded into the p-well area and the base width of the NPN/PNP bi-pole parasitically generated in SCR was expanded to reduce the current gain (Beta) and thus raise holding voltage. In addition, a resistant role on a discharge path was designed by covering the cathode phase with n-well and inserting a well-resistor, and the emitter injection efficiency of the parasitic NPN bipolar was reduced to raise the holding voltage. The operation principle of the proposed device is as follows: When ESD phenomenon occurs from the anode electrode, the junction of the n-well and the p-well is reverse biased. At this moment, avalanche break down occurs due to high electric field between the junctions. And EHP (Electron-Hole Pair) is generated by avalanche breakdown, when hole current flows to p-drift junction through parasitic PNP bipolar Q2, currnt of Q2 causes a voltage drop in Rn2 and the p-well electric potential increases. The emitter-base junction of parasitic NPN bipolar Q3 becomes forward-biased due to the raised electric potential of the p-well, and NPN bipolar Q3 turns on. When Q3 turns on, Q3 current causes a voltage drop in Rn1, and PNP bipolar Q1 also turns on. Q1 current also results in a voltage drop at Rp, which helps Q3 turn on. In this process there is no need to supply bias to Q3 any longer due to Q3 current. The holding voltage of the ESD protection device relies on the space charge neutralization in the base area between NPN and PNP due to the carrier inflowing from the NPN/PNP bipolar emitter area. Thus, the bipolar base width and the p-drift area width are very important. To Analyze holding voltage properties associated with this, design parameters D1, D2 and D3 have been set. Individual design parameters include floating n+ area (D1) associated with PNP bipolar transistor base width, p-drift junction length (D2) associated with NPN bipolar transistor base width, Distance (D3) between edge of Nwell and edge of floating N+ area in Nwell and Distance (D3) between edge of Pwell and edge of P-drift area in Pwell associated with PNP/NPN bipolar transistor base width (shown in Figure. 4).

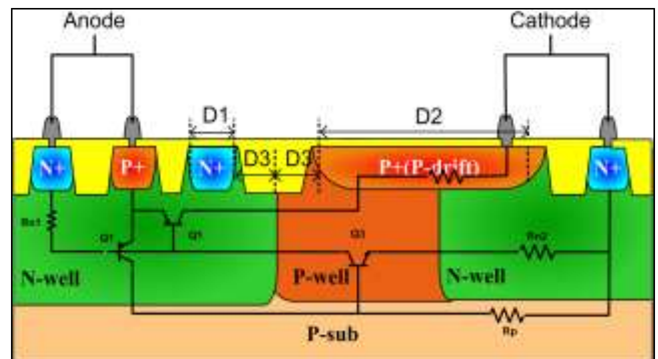


Figure 4. Cross section of the proposed SCR-based ESD protection device

3. SIMULATION RESULTS

3.1 I/O Clamp ESD protection device

They are investigated by using the Synopsys TCAD simulator Simulation results for trigger voltage, holding voltage and turn-on time are shown in Table I.

The conventional GGNMOS has high trigger voltage of 7.69V, STNMOS_PMOS and proposed STNMOS_PNP has low trigger voltage about 5V. There are shown Figure 5.

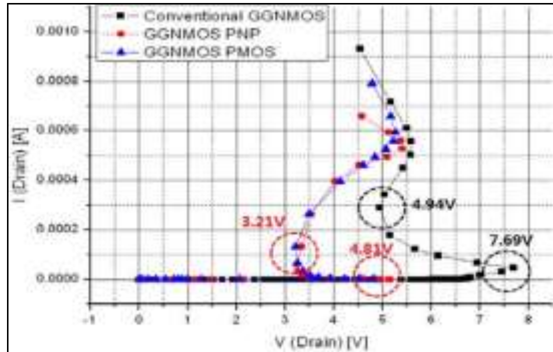


Figure. 5. Simulated I-V curve characteristics of the conventional GGNMOS, conventional STNMOS and proposed STNMOS

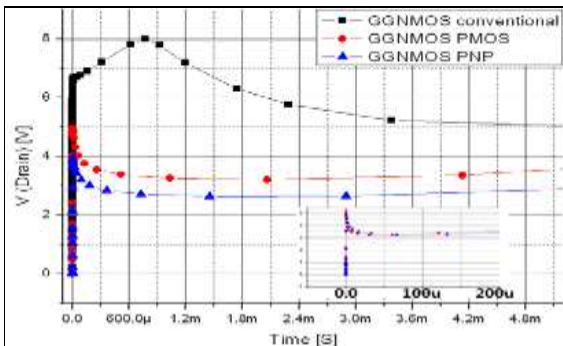


Figure. 6. Turn-on waveform of the conventional STNMOS and proposed STNMOS.

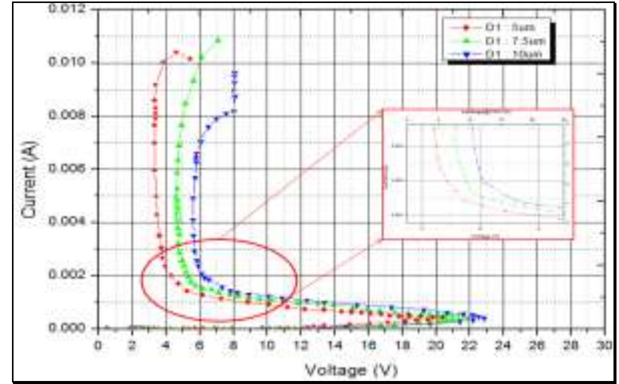
The comparisons of turn on times between the conventional STNMOS and proposed under 10V voltage. The turn-on time of the STNMOS_PNP (~30us) is faster than that of the STNMOS_PMOS(~60us). There are shown Figure 6. As a result, the proposed STNMOS will quickly discharge ESD current.

Table 1. Simulation Results of The Proposed Device

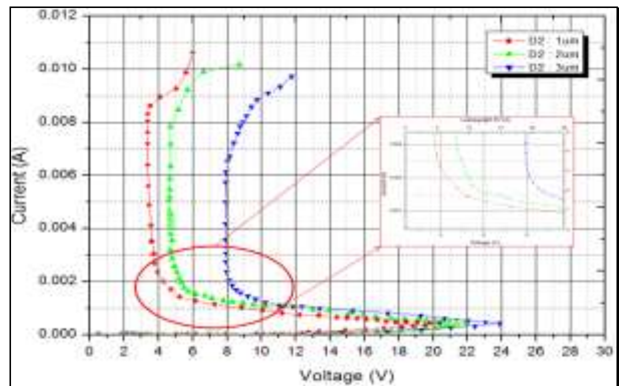
	Trigger Voltage(Vt)	Holding Voltage(Vh)	Turn-on Time
Conventional GGNMOS	7.69 V	4.94 V	290us
GGNMOS(PMOS)	4.81 V	3.21 V	60us
GGNMOS(PNP)	4.81 V	3.21 V	30us

3.2 Power Clamp ESD protection device

SCR-based device with high holding voltage can be composed, we tried to analyze the holding voltage trend of the single SCR-based ESD protection device with different design parameters, D1, D2 and D3 (shown in Figure. 4). They are investigated by using the Synopsys TCAD simulator



(a)



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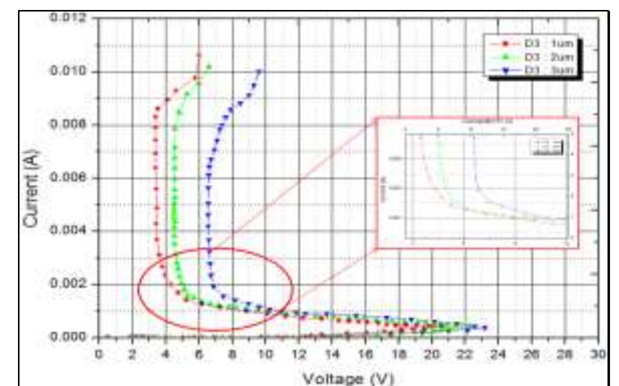

(c)

Figure 7. The Simulated I-V characteristics of a single SCR-based device with different design parameters of (a) D1 variation, (b) D2 variation and (c) D3 variation

All the design parameters of a SCR-based device in the simulation are fixed at a similar value except the design parameters D1, D2 and D3. The simulated I-V characteristics of a single SCR-based device with different design parameters are shown in Figure 4(a). The graph in Figure 7(a) indicates length changes in the graph design parameter D1: 5um, 7.5um and 10um. The more the design parameter D1 increases, holding voltages increased up to 3.3V, 4.7V and 5.6V, respectively, as current gains decreases with the increases in the base width of the PNP bipolar. Figure 7(b) show a graph when the design parameter D2 changes in length : 1um, 2um and 3um. As the design parameter D2 gradually increases, the holding voltage increases from 3.3V to 7.9V with the decrease in current gain. Figure 7(c) is graph showing length changes in design parameter D3 : 1um, 3um and 5um. As the design parameter D3 gradually increases, the holding voltage increase from 3.3V to 6.5V with the increase in NPN/PNP bipolar base width. Simulation results for trigger voltage and holding voltage are shown in Table II.

Table 2. Simulation Results of The Proposed device

D1	**Trigger Voltage(Vt)**	**Holding Voltage(Vh)**
5 um	20.5 V	3.3 V
7.5 um	21.8 V	4.7 V
10 um	22.9 V	5.6 V
D2	**Trigger Voltage(Vt)**	**Holding Voltage(Vh)**
1 um	20.5 V	3.3 V
2 um	21.8 V	4.8 V
3 um	23.8 V	7.9 V
D3	**Trigger Voltage(Vt)**	**Holding Voltage(Vh)**
1 um	20.5 V	3.3 V
3 um	22.1 V	4.5 V
5 um	23.1 V	6.5 V

4. CONCLUSION

In this paper, the substrate triggered NMOS and SCR based ESD protection device for I/O and power clamp is proposed. The proposed substrate triggered NMOS devices have faster turn on time(~30us) than conventional substrate triggered NMOS. Also, proposed SCR-based device with a high holding voltage for a latch-up immune high voltage application. In TCAD simulation results, the holding voltage of the proposed SCR-based device changes from 3.3 V to 7.9V. Consequentially, the proposed ESD protection devices can provide improved performance for I/O and power clamp.

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