A Low Power Analog to Digital Interface for Digitally Controlled DC-DC Converter

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Abstract: This paper presents a novel low power analog to digital interface (ADI) for digitally controlled DC-DC converter. The whole ADI has been implemented in commercial 0.18 μm CMOS process design kit. Simulation results validate the design concept. The proposed ADI consumes 7.5 μA current under 1 V supply voltage with 500 KHz sampling rate and 4-bit resolution. It is very suitable for digitally controlled pulse width modulation (PWM) mode DC-DC converter.

1. Introduction

Efficient, high quality smart power management modules are required in reliable, portable devices and for longer battery life. Digitally controlled DC-DC converter topology offers power supply designers such a possible solution. Such DC-DC converter converts the error signal into digital signal and then through PID controller to define the control transfer-function in digital domain, which further controls the output power train. The digital control technique makes the communication between power management module and microprocessor of the mobile devices become more convenient, and results in a more flexible and tunable power control loop. Recently, research literatures in digitally controlled PWM mode and dual-mode DC-DC converters were presented [1], [2]. In order to achieve high efficiency in the digitally controlled DC-DC converter design, low power high speed ADI is required. Literatures [3], [4] presented some ADIs based on voltage controlled oscillator (VCO) and delay line, and [2] also reported a ring-oscillator type ADI. This paper proposes a novel charge pump counter based ADI, which has relatively lower power consumption.

2. Charge Pump Counter Based ADI

The proposed ADI uses a charge pump based voltage-to-time converter to convert input voltage difference into time difference. A counter is used to digitalize the time difference. Fig. 1 shows the simplified circuit of the voltage-to-time converter. At stable status, the Q of the converter output is "0". Suppose a rising edge at the CLK terminal triggers Q to "1", then the switch S1 is turned off, V_A is disconnected with ground, the precise current source I_C starts to charge capacitor C_C, once V_A reaches V_{IN}, the amplifier outputs a high level, through the inverter, and then resets the D flip-flop. There is a positive pulse presented at Q, once a rising edge triggers the D flip-flop. The ON time of the positive pulse presented at Q is:

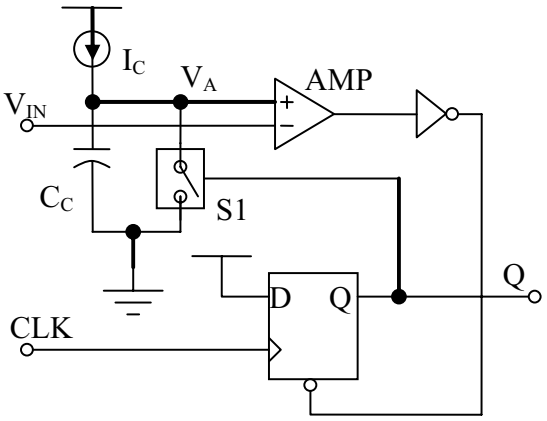

Figure 1. The Voltage-to-Time Converter.

$$T_{ON} = \frac{C_A V_{IN}}{I_C} + T_{AMP} + T_D \quad (1)$$

$$= \frac{C_C + C_{AMP} + C_{S1} + C_{IC}}{I_C} V_{IN} + T_{AMP} + T_D, \quad (2)$$

where C_A is the total capacitance at node V_A, C_{AMP} is the amplifier input capacitance, C_{S1} is the parasitic capacitance of the CMOS switch S1, and C_{IC} is the parasitic capacitance of the precise current source I_C. T_{AMP} is the delay time of the amplifier and T_D is the delay time from the amplifier output to the Q of the D flip-flop.

The proposed ADI is presented in Fig. 2. Two identical voltage-to-time converters generate two positive pulses (T_{ON+}, T_{ON-}) which are triggered by the same rising edge of F_S whereas the ON time is controlled by V_{IN+} and V_{IN-} respectively. As demonstrated in Fig 3, the difference of T_{ON+} and T_{ON-} are generated by an XOR gate, and the difference of the ON time (ΔT_{ON}) is:

$$\Delta T_{ON} = t_3 - t_2 \quad (3)$$

$$= \frac{C_A}{I_C}\left(V_{IN+} - V_{IN-}\right) \quad (4)$$

$$\approx \frac{C_C}{I_C}\Delta V_{IN} = K_C \Delta V_{IN}, \quad (5)$$

where K_C is the gain of the voltage-to-time converter.

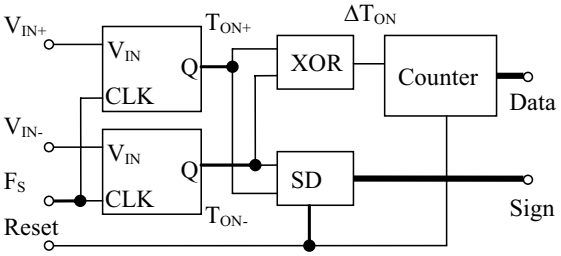

Figure 2. The Analog to Digital Interface.

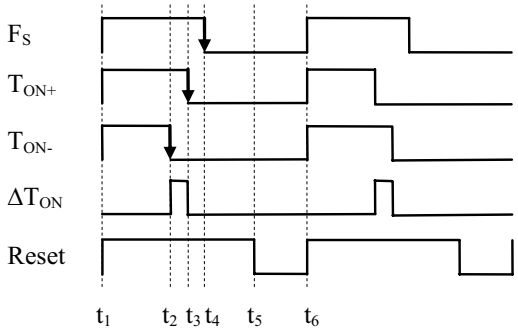

Figure 3. The Timing of the Analog to Digital Interface.

As the parasitic capacitances C_{AMP}, C_{S1} and C_{IC} present nonlinear capacitance when V_A is varied during the charging period, C_C is chosen large enough to dominate the capacitance at node V_A. Thus, the effects of the parasitic capacitances are neglected and the time difference ΔT_{ON} is proportional to the input voltage difference ΔV_{IN}.

The counter in Fig. 2 uses ΔT_{ON} as a time window to count a high frequency clock (F_C). At the end of one conversion cycle, the value of the counter presents the input voltage difference in digital domain. Due to XOR gate removes the sign of the voltage difference, a sign detector (SD) modified from conventional three-status phase frequency detector (PFD) is used to generate a 2-bit sign signal, which tells the PID controller the sign of the original input voltage difference (ΔV_{IN}). Fig. 4 draws the diagram of such SD and Fig. 5 shows the timing of the SD. The function table of the SD is shown in Table 1.

The counter in Fig. 2 can be totally realized by basic digital gate and D flip-flop. Fig. 6 presents its diagram. The AND gate makes the counter only count the clock F_C within the time window ΔT_{ON}, and hold the value until the reset signal comes. The 5-bit counter is realized by so called true single phase D flip flop (TSPDFF). The reset is valid when a low level presents at the reset terminal. From Fig. 3, the timing of the ADI can be demonstrated. During the design, the conditions $t_2>t_1$ and $t_3<t_4$ are strictly adhered. Thus, the analog to digital conversion will be complete in the positive half cycle of F_S. The counter holds its value after t_3. The falling edge at t_4 is used to trigger PID controller to read the conversion result of the counter and SD. According to the counter and SD outputs, PID controller will get the right information of the input voltage difference in digital domain. The reading process is complete before t_5. Subsequently, the negative pulse between t_5 and t_6 of the reset signal resets the counter and SD before the next conversion cycle. Its reset window (t_6-t_5) is one fourth of the full cycle of F_S. The reset signal and Fs signal are generated by a divide-by-2 circuit and logical gate from the same reference clock F_{REF} which has 2 times frequency of F_S.

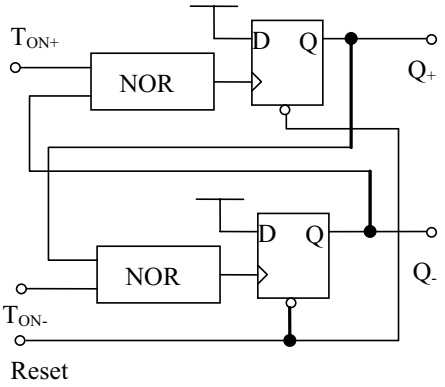

Figure 4. Falling edge SD.

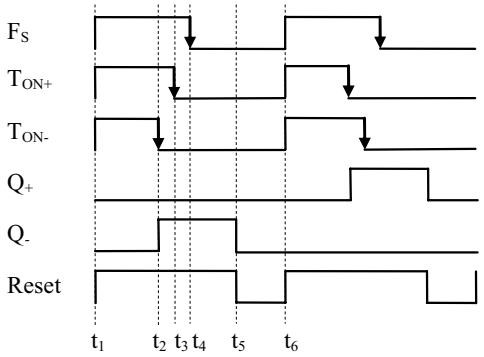

Figure 5. The Timing of SD.

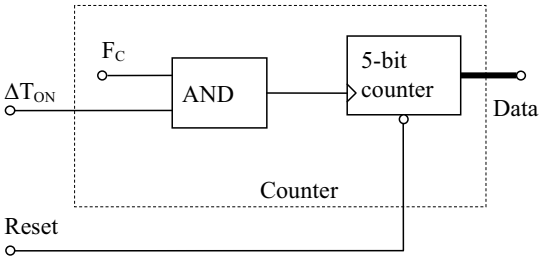

Figure 6. The 5-bit Time Windowed Counter.

Table 1 SD Function Table

Q_+Q_-	Sign
00	F_S Over Speed
01	$\Delta V_{IN} > 0$
10	$\Delta V_{IN} < 0$
11	$\Delta V_{IN} = 0$

The proposed ADI only uses one counter to count the high frequency clock in very short time window; hence the power consumption is highly reduced. Due to the symmetric structure of the ADI, the effect of the amplifier

systematic offset and the time delay of the digital blocks in Fig. 1 can be eliminated by the XOR operation. The time difference is only related on the charge current I_C, holding capacitor C_C and the input voltage difference ΔV_{IN}.

3. Simulation Result

The proposed ADI has been implemented in transistor level in 0.18 µm CMOS process. The charging current source I_C is realized by highly matched wide swing current mirror. A 10 nA PTAT current reference circuit [5] is used to provide reference current. The amplifier of the voltage-to-time converter is realized by a conventional OTA with rail-to-rail input stage. The hold capacitor C_C is a high quality MIM capacitor. The digital blocks are designed by using true single phase type logical circuits.

The input range of the ADI is mainly determined by the input common mode range of the amplifier inside the voltage-to-time converter. In this design it is rail-to-rail. The quantization resolution is controlled by the voltage-to-time converter gain K_C. The final resolution is also determined by the counter resolution.

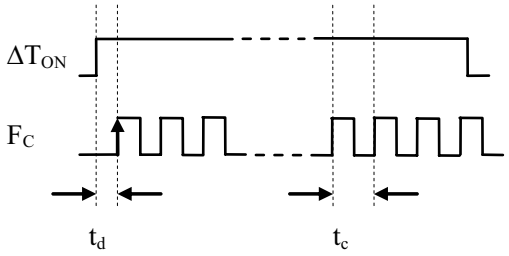

Figure 7. Time Window of the Counter.

As Fig. 7 shown, due to the high frequency clock F_C and the time window ΔT_{ON} are not synchronized, there is a random time delay t_d between the time window and the first clock rising edge.

In case that F_C and ΔT_{ON} are synchronized, the ideal output of the counter is:

$$D_0 = \left[\frac{\Delta T_{ON}}{t_c} \right], \tag{6}$$

where [x] denotes a floor function. This function returns the maximum integer which is less than the float number x. t_c is the period of F_C.

In case that F_C and ΔT_{ON} are not synchronized, the practical output of the counter due to t_d is:

$$D = \left[\frac{\Delta T_{ON} - t_d}{t_c} \right], \quad 0 \le t_d < t_c \tag{7}$$

Rewrite ΔT_{ON} and t_d as

$$\Delta T_{ON} = Kt_c + nt_c, \; 0 \le n < 1 \tag{8}$$

$$t_d = dt_c, 0 \le d < 1, \tag{9}$$

where K is a non-negative integer number, n and d are two random variables, which have the random value between 0 and 1.

From (6) to (9), the counter output can be

$$D_0 = K \tag{10}$$

$$D = K + [n - d] \tag{11}$$

$$\Delta D = D - D_0 = \begin{cases} -1, & d > n \\ 0, & d \le n \end{cases} \tag{12}$$

Eqn. (12) shows that, in the case that using M-bit counter to achieve (M+1)-bit resolution ADI, the maximum Differential Nonlinearity (DNL) error caused by the random delay t_d is 1 LSB (Since the counter only counts half of the input full scale, the SD gives the ADI one more bit resolution than the counter.). Such a DNL may cause the ADI has missing code error [6]. Fig. 8 shows the simulated missing code error for using 3-bit counter to achieve 4-bit ADI.

In order to solve this problem, the counter may have higher resolution. In this design, a 5-bit asynchronous counter is used for the 4-bit ADI. This guarantees the final ADI DNL is always less than 1/4 LSB. The ADI is monotonic and has no missing code error. Fig. 9 shows the simulated 10 runs of the conversion curves.

The current consumption of the ADI highly depends on the input voltage difference ΔV_{IN}. A larger ΔV_{IN} results in a larger ΔT_{ON}, a longer counting time for the counter, hence more current consumption. To evaluate the current consumption properly, the proposed ADI is simulated over 15 conversion cycles. These 15 conversion cycles cover and only cover the full set of the output code bins. The current consumptions of these 15 conversion cycles are averaged to get the final current consumption of the ADI. In this design, it is 7.5 µA.

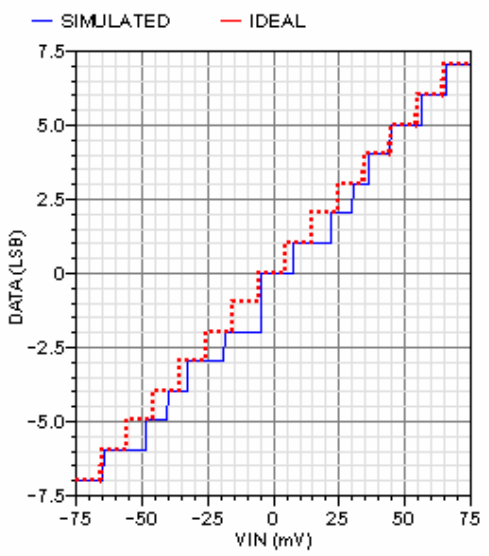

Figure 8. The Simulated Missing Code Error for Using 3-bit Counter to Achieve 4-bit ADI.

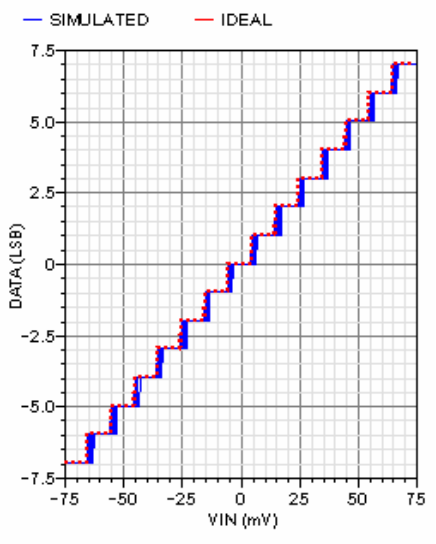

Figure 9. The Simulated 10 Runs of the Conversion Curves.

In digitally controlled DC-DC converter application, the V_{IN+} of the ADI is connected to converter output V_{OUT}, the V_{IN-} is connected to an arbitrary reference voltage V_{REF}. When the converter is working, V_{OUT} is regulated around V_{REF}. Hence it is not necessary to make the quantization window of the ADI cover from ground to supply voltage. The ADI should be monotonic, but need not have very good linearity. Thus the desired ADI should have fast speed, low power consumption, suitable quantization window and small quantization size. In this design, the ADI sampling rate (conversion time) is 500 KHz (2 µS). The quantization window is 150 mV, which is enough for the DC-DC converter output ripple. The quantization size is 10 mV. Table 2 shows the comparison between this work and the references.

4. Conclusion

The paper presents a novel low power ADI for digitally controlled DC-DC converter. The proposed ADI has been simulated under 1 V supply voltage in 0.18 µm CMOS process. The average current consumption of the ADI is 7.5 µA with 500 KHz sampling rate and 4-bit resolution.

Table 2. Comparison of the ADIs

	[4]	**[2]**	**This Work**
Process	0.5 µm	0.25 µm	0.18 µm
Sampling Rate	1 MHz	500 KHz	500 KHz
ADI Type	Delay Line	Ring Oscillator	Charge Pump Counter
Quantization Size	50 mV	16 mV	10 mV
Quantization Window	450 mV	80 mV	150 mV
Current Consumption	-	37 µA	7.5 µA
Supply Voltage	5 V	2.75 V	1 V

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