An Inductor-type Current-Mode Buck Converter For Mobile Applications

Youngkook Ahn, Donghun Heo, Hyunseok Nam, and Jeongjin Roh
Department of Electrical Engineering, Hanyang University
Ansan 426-791, Korea
Tel: +82-31-400-5168, Fax: +82-31-501-5622
E-mail: jroh@hanyang.ac.kr

***Abstract*—An inductor-type current-mode DC-DC buck converter was evaluated through HSPICE simulation with 0.18μm CMOS process parameters. The current programmed mode (CPM) controller is designed for improved controllability of the DC-DC converter. A DC-DC buck converter is able to operate from 2.5V to 3.3V supply voltage. Overall peak efficiency is about 92$\%$.**

I. INTRODUCTION

IN TODAY'S consumer market, battery-operated portable electronic devices such as cellular phones, MP3 players, personal digital assistants (PDAs) and other devices are in great demand. Therefore, there is a need for low-voltage high-efficiency DC-DC buck converters, which are suitable for single-cell battery systems to maximize the operation time and to minimize the physical size for portable devices. The design of low-voltage high-efficiency DC-DC buck converter thus becomes challenging and important research since the designs of the required analog building blocks with acceptable performance are very difficult [1].

Fig.1 shows the block diagram of a current-mode buck converter. The buck converter consists of a monolithic controller and several external passive components. Usually, the large inductor and capacitors are used as off-chip components. Apart from those passive components, other circuit blocks can be implemented on-chip. The clock generator produces a clock signal that sets the SR latch, which in turn sets the PMOS and NMOS power transistors. The reset timing of the converter is determined by the comparator, which compares the measured inductor current with the compensated control signal [3].

This paper proposes a current-mode DC-DC buck converter for mobile applications. An inductor-type current-mode DC-DC buck converter was evaluated through HSPICE simulation with 0.18μm CMOS process parameters. In Section II, the controller circuit used in the current-mode DC-DC buck converter is examined in detail, performance of the converter is evaluated based on the simulation result in Section III, Finally, the conclusion of the paper is presented in Section IV.

II. CONTROLLER DESIGN

A. Error Amplifier and Compensator

An inductor-based switching DC-DC converter is a nonlinear circuit that operates according to the switching mechanism.

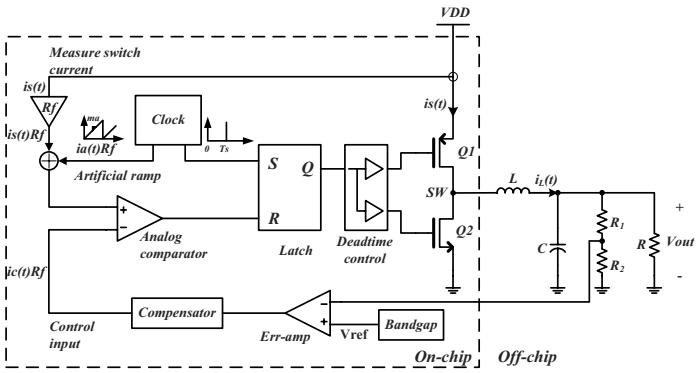

Fig. 1. Block diagram of a current-mode buck converter.

A linear small signal model is required to analyze the stability of the converter circuit's feedback loop. A typical voltage mode DC-DC buck converter has two poles and can be generally modeled as a second-order equation, as follows

$$G_{vd}(s) = \frac{V}{D} \cdot \frac{1}{(1 + (\frac{L}{R}) \cdot s + LC \cdot s^2)}. \qquad (1)$$

Equation (1) indicates the control-to-output transfer function G_{vd}. Here, D denotes the ratio of high region with a PWM wave. A current mode DC-DC buck converter also has two poles. However, the second pole of a current mode DC-DC buck converter is located near the switching frequency away from the dominant pole and hardly affects overall system stability [4], [5], [6]. Therefore, the model can be approximated into a first-order equation with a single pole. Control-to-output transfer function G_{vc} of the first-order model can now be expressed as

$$G_{vc}(s) = \frac{V_{out}(s)}{i_c(s)} = \frac{1}{(1 + s \cdot RC)}. \qquad (2)$$

With one less dominant pole, the current mode converter has an advantage over the voltage mode converter in terms of being better able to secure stability [1], [2], [3].

Fig. 2 displays the converter frequency characteristics of G_{vc} based on the more accurate equation. As the graph indicates, while the phase margin of the converter is sufficient, the gain is very low. In turn, a proportional-plus-integral (PI) compensator was used to compensate for the low gain [5].

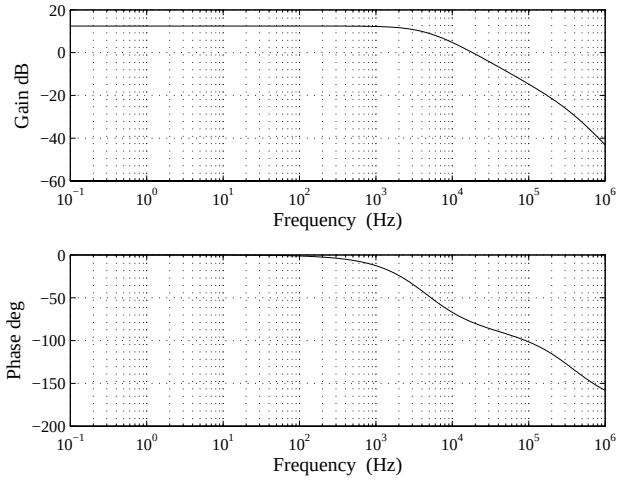

Fig. 2. Frequency characteristics of uncompensated buck converter.

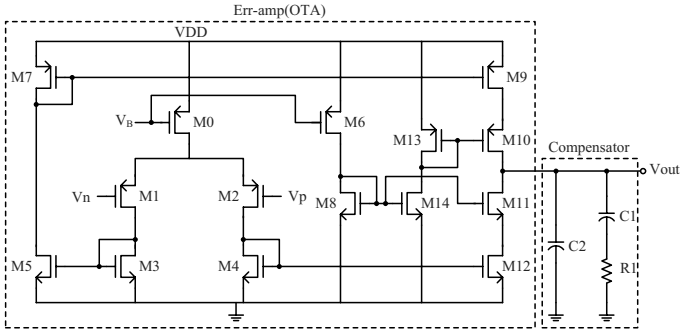

Fig. 3. Error amplifier and compensater.

The first thing that must be determined for designing the compensator is the unit gain frequency. Subsequently, the amount of compensation can be set for the gain or phase. The unit gain frequency is usually set below 1/10 of the converter's switching frequency. Otherwise, the compensator gain becomes too high near the switching frequency, and the compensator ends up amplifying the switching harmonics that occur around the switching frequency, ultimately affecting the converter's internal operation [3].

Once the unit gain frequency is established, the pole and zero frequencies of the compensator and the gain at the unit gain frequency are determined. A point to note here is that the mid-point between the pole and zero frequencies must coincide with the unit gain frequency to prevent the phase margin from decreasing.

Fig. 3 exhibits the circuit diagram consisting of the conventional PI compensator and the operational transconductance amplifier (OTA) used as the error amplifier. This type of compensator is often used to compensate for a low open-loop gain of a system with a sufficient phase margin. Two capacitors and one resistor in Fig. 3 create a pole and a zero, respectively, as follows

$$f_z = \frac{1}{2\pi R_1 C_1} \tag{3}$$

$$f_p = \frac{C_1 + C_2}{2\pi R_1 C_1 C_2} \approx \frac{1}{2\pi R_1 C_2} \; where \; C_2 \ll C_1. \tag{4}$$

The compensator gain that includes the pole and the zero at the converter's unit gain frequency is

$$A_v = g_m R_1 \tag{5}$$

The frequency characteristics of the PI compensator's transfer function G_c according to the pole and the zero are shown in Fig. 4. Here, g_m is OTA's transconductance. The resistor R_1 and the capacitors C_1 and C_2 used for the compensator are integrated onto the chip. Fig. 5 illustrates the frequency characteristics of the total loop of the designed current-mode DC-DC buck converter with the compensator. We were able to achieve sufficient DC gain and phase margin by compensating the gain and the phase properties of G_{vc}.

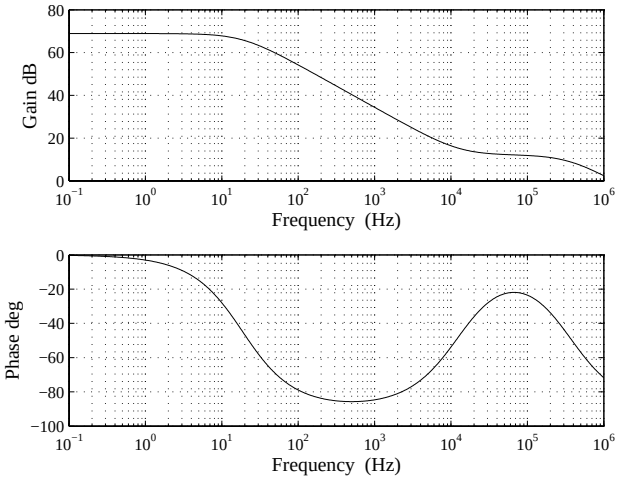

Fig. 4. Frequency characteristics of compensator.

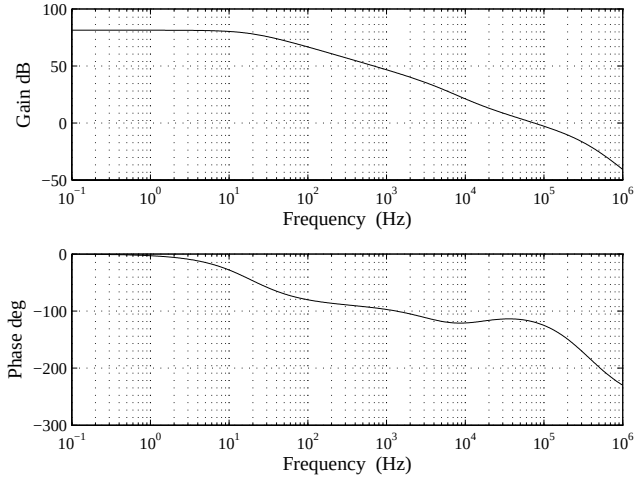

Fig. 5. Frequency characteristics of compensated buck converter.

B. Clock and Ramp Generator

The control signal of a current-mode DC-DC converter that controls the entire converter using the inductor current is sensitive to disturbance. When the current-mode DC-DC buck converter is operating with a duty of 0.5 or less, disturbance does not affect overall converter operation. However, at a duty greater than 0.5, the effect of disturbance increases with the repetitions of the switching period. This results in oscillation of the control signal, which disables normal converter operation. In order to prevent such oscillation caused by disturbance, an artificial ramp with a certain slope is added to the control signal of the current sensing circuit. The artificial ramp signal prevents oscillation caused by disturbance even when the converter operates with a duty greater than 0.5. The slope of the artificial ramp signal m_a is a very significant factor for securing stability. The value of m_a is generally determined as follows [3]

$$m_a \geq \frac{m_2}{2}. \tag{6}$$

where m_2 denotes the slope V_{out}/L in the region where inductor current decreases.

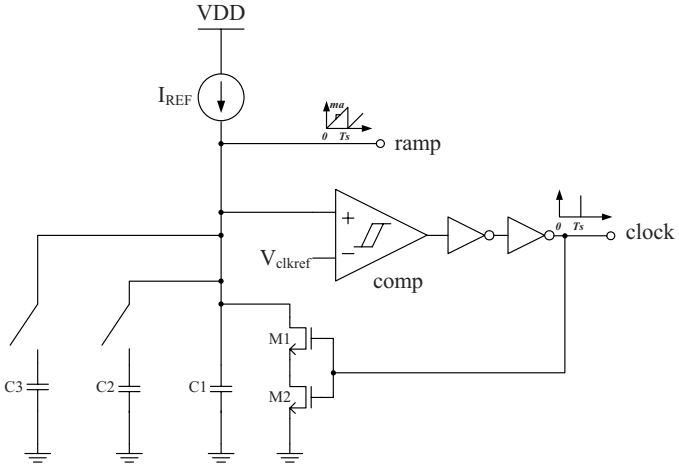

Fig. 6. Clock and ramp generation circuit.

Fig. 6 is the circuit for generating the artificial ramp signal and the clock signal. The slope of the artificial ramp is determined by I_{REF} and C_1. When I_{REF} from the current source charges the capacitor C_1, the voltage at the ramp node increases at a fixed rate I_{REF}/C_1, which is equal to the slope m_a. The ramp voltage can be expressed as follows

$$ramp = \frac{I_{REF}}{C_1} \times t. \tag{7}$$

If the increasing ramp signal reaches V_{clkref}, the output node of the hysteresis comparator switches from low to high and the clock also becomes high. Once the clock switches to the high state, it turns on transistors M_1 and M_2. In turn, C_1 is discharged and the ramp node voltage decreases. The discharging causes an instantaneous jump in the amount of current, and transistors M_1 and M_2 are linked in series to prevent any sudden current inrush to the transistors. When the ramp node voltage decreases to the low boundary of the hysteresis comparator, its output switches from high to low, the clock drops to the low state, and M_1 and M_2 are switched off, triggering I_{REF} to charge C_1. Repetitions of this mechanism generate the clock signal, which synchronizes and generates the ramp signal. The clock frequency becomes the converter's switching frequency. C_2 and C_3 are capacitors for adjusting the frequency by trimming if the clock frequency drifts away after actual chip implementation.

III. Simulation Results

The HSPICE simulation results are shown in this section with $0.18\mu m$ CMOS process. The V_{TH} of the NMOS and PMOS were $V_{THN} \approx$ 0.75V and $V_{THP} \approx$ -0.71V, respectively. Fig. 7 represents the waveforms of the output signal and the SW node signal. A supply voltage of 3.3V was applied to the converter and the output voltage was set to 1.2V. The switching frequency was set at 1.25MHz.

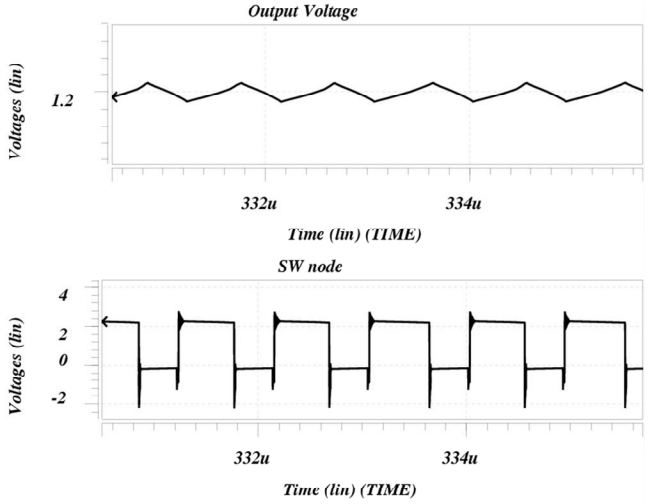

Fig. 7. Output voltage and SW signal

Fig. 8 displays the output voltage and inductor current waveform according to variation in the load current. The step response of the output voltage was measured as the load current was varied $100mA \rightarrow 400mA \rightarrow 100mA$. The measured overall peak efficiency of the current mode DC-DC buck converter proposed in this paper is about 92%. Table I summarizes the performance of the current-mode DC-DC buck converter implemented in this paper.

TABLE I
SIMULATION RESULTS OF THE DC-DC BUCK CONVERTER

Technology	standard 0.18 μm CMOS
Switching frequency	1 $\sim$ 1.5 MHz
Efficiency	Max 92 %
Input voltage range	2.5V $\sim$ 3.3V
Output voltage range	0.5V $\sim$ Input voltage
Load current range	maximum 400mA
Quiescent current	440 μA
Line regulation	8.63 mV/V @ (load 50mA)
Load regulation	0.13 mV/mA @ (V_{DD} 3.3V)

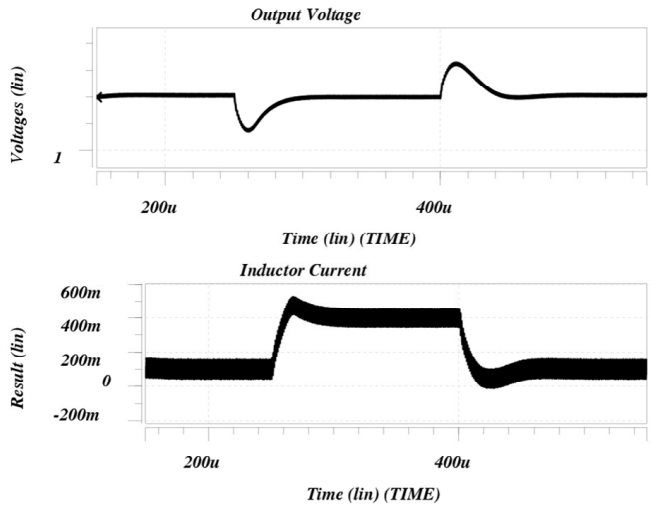

Fig. 8. Load variation of 100mA to 400mA, then back to 100mA

IV. Conclusion

This paper proposed a current-mode DC-DC buck converter for mobile applications. An input voltage range of this work is from 2.5V to 3.3V, the switching frequency is from 1MHz to 1.5MHz, the maximum of load current range is 400mA. We were able to achieve a peak efficiency of over 92%.

Acknowledgements

This work was supported by the IT-SoC Promotion Center of ETRI, Korea.

References

[1] C. Y. Leung, P. K. T. Mok, K. N. Leung, and M. Chan, "An integrated CMOS current-sensing circuit for low-voltage current-mode buck regulator," *IEEE Trans. on Circuits and Systems-II*, vol. 52, pp.394-397, Jul. 2005.

[2] M. Brown, *Practical Switching Power Supply Design*, San Diego, CA: Academic, 1990.

[3] R. W. Erickson, and D. Maksimovic, *Fundamentals of power electronics*, 2nd edition, KAP, 2001.

[4] R. Middlebrook, "Modeling current-programmed buck and boost regulators," *IEEE Trans. Power Power Electronics*, vol. 4, pp. 36-52, Jan. 1989.

[5] I. Pressman, *Switching Power Supply Design*, 2nd ed. New York: McGraw-Hill, 1998.

[6] P. T. Krein, *Elements of Power Electronics*, New York, NY: Oxford Univ. Press, 1998.