An Ultra-Low Power and High Resolution Digitally Controlled Oscillator with Gain Estimation Technique for Direct Modulation

Seong-Jin Oh[1], Hamed Abbasizadeh[1], Sang-Sun Yoo[2], and Kang-Yoon Lee[1]
[1] College of information and Communication Engineering, Sungkyunkwan University,
2066,Seobu-ro Jangan-gu, Suwon, Korea
[2] Department of Electrical Engineering, KAIST University Daejeon, 305-732, Korea
E-mail: geniejazz@skku.edu, hamed@skku.edu, rapter@kaist.ac.kr, klee@skku.edu

Abstract: This paper presents an ultra-low power and high resolution Digitally Controlled Oscillator (DCO) with gain estimation technique for direct modulation. Three capacitor banks and Delta Sigma Modulator (DSM) are adopted for ultra-high resolution and for the low current consumption, 0.7 V of supply voltage is adopted. Gain estimation technique is adopted for direct modulation. The proposed DCO is designed and fabricated using 55 nm CMOS process and its oscillation Frequency is 4.8 GHz. 1-bit resolution of MSB, LSB, and Fine cap banks are 81.92 MHz, 5.12 MHz, 153.6 kHz, respectively, the nominal phase noise at 1 MHz offset is -116.28 dBc/Hz, and the current consumption is 850 uA when 0.7 V VDD is supplied.

Keywords-- **All-Digital Phase Locked Loop, Digitally Controlled Oscillator, Gain Estimation, Direct Modulation**

1. Introduction

Demands of low power transceiver are increasing with the development of Internet of Things (IoT) devices in recent years. All Digital Phase Locked Loop (ADPLL) is the most suitable PLL type for implementing low power RF Transceiver since the most of blocks are implemented in digital circuits. The most important role of PLL in Frequency Shift Keying (FSK) system is to send data to Receiver (Rx) by changing its local frequency in certain deviation ratio. DCO is the main block which generates the local frequency of the ADPLL.

In conventional FSK Transmitter (Tx), modulating frequency can be done only by PLL which is an closed-loop system. The accuracy of the frequency is really high, however, its bandwidth has certain limit to follow the Tx data pattern which limits overall speed of data rate.

By gain estimation technique proposed in this paper, direct modulation can be done using only DCO itself by changing its fine cap bank code. Moreover, since the modulation is using only DCO, current consumption is much lower than that of using closed phase-locked loop.

2. Main Architecture of the Proposed DCO

2. 1 Overall Architecture

Figure 1 shows the overall architecture of the proposed DCO. PMOS and NMOS cross-coupled structures are designed for negative gm with MOSFETs of M1, M2, M3, and M4. Three capacitor banks and DSM are adopted for ultra-high resolution. Three cap. banks are consist of MSB, LSB, and Fine cap banks. 5-bit DSM is adopted in the proposed DCO for dithering fine capacitor and makes the resolution 5 times higher than the original fine capacitor bank resolution. Lastly, gain estimation block is adopted for estimating 1-bit fine cap. resolution.

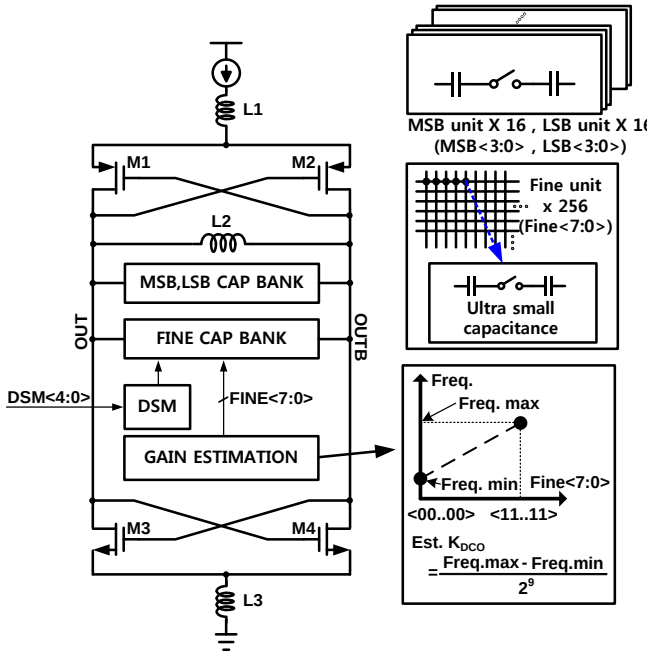


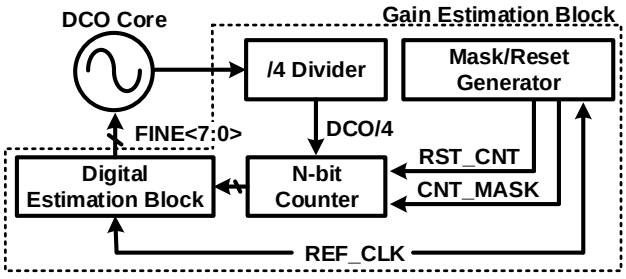
Figure 1. Overall Architecture of the proposed DCO

2. 2 Gain Estimation Technique

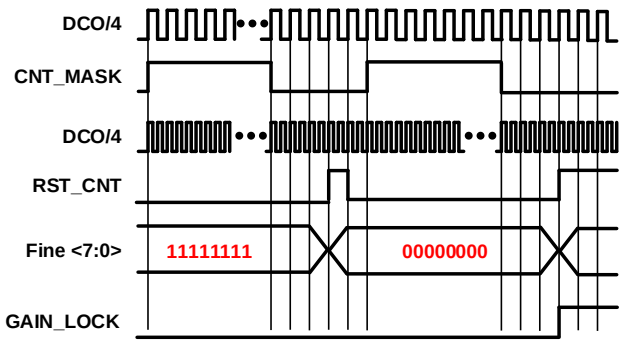
The gain estimation technique is to estimate the 1-bit fine capacitor resolution. It is essential to modulate the frequency only by DCO so that direct modulation becomes possible.

Figure 2 shows the block diagram of the proposed gain estimation block and its timing diagram. It consists of Divided by 4 Divider, Mask/Reset Generator, N-bit Counter, and Digital Estimation Block (DEB). Mask/Reset Generator generates the certain mask, CNT_MASK, from the reference clock, REF_CLK. CNT_MASK becomes the enable signal of N-bit counter so that divided by 4 DCO clock can be counted while CNT_MASK is high. When CNT_MASK becomes low, reset of the counter, RST_CNT, becomes high for the certain duration so that the output of counter can be delivered to the DEB and the counts becomes '0'. When gain estimation begins, DEB outputs the FINE<7:0> to all high at the first counting, and all low at the second counting. After second counting, GAIN_LOCK becomes high and gain estimation is over.

From the count difference between the first counting and the second counting, DEB calculates the count difference with the duration of CNT_MASK, and 1-bit fine cap. resolution can be determined by the equation (1).



(a)



(b)

Figure 2. (a) Block Diagram of Gain Estimation Block (b) Timing Diagram of Gain Estimation Block

$$\Delta F = \frac{Frq_{max} - Frq_{min}}{2^{8}\,(\text{Fine bits})} = \frac{(cnt_{max} - cnt_{min})/Frq_{CNT\_MSK}}{2^{8}\,(\text{Fine bits})} \quad (1)$$

ΔF denotes the 1-bit resolution of fine cap., Frq_{max} denotes the maximum frequency of DCO, Frq_{min} denotes the minimum frequency of DCO, cnt_{max} denotes the maximum counting value, cnt_{min} denotes the minimum counting value, and Frq_{CNT_MSK} denotes the frequency of CNT_MASK.

3. Simulation Results

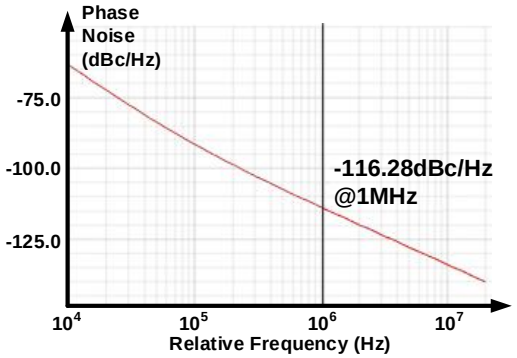
Figure 3 (a) shows the phase noise results of the proposed DCO. As can be seen from the results, the phase noise of the proposed DCO is -116.28 dBc/Hz when the oscillation frequency is 4.8 GHz.

Figure 3(b) shows the direct modulation result after gain estimation. When Data Enable becomes high, than frequency of DCO starts to modulate by Tx data. Tx data changes with the frequency of 500 kHz so that the data rate is 1 Mbps. Since the deviation ratio was set as 500 kHz, gain estimation block calculates the 1-bit fine cap resolution and set the fine cap code which makes 500 kHz difference.

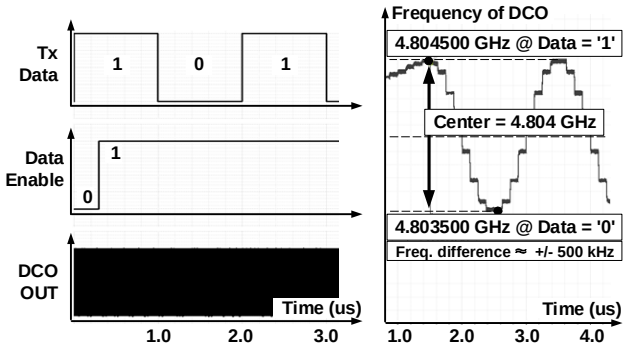
4. Conclusion

This paper presents an ultra-low power and high resolution DCO with gain estimation technique. Gain estimation technique is adopted to estimate the 1-bit fine cap. resolution for direct modulation.

The proposed DCO is designed and fabricated using 55 nm CMOS process and its oscillation frequency is 4.8 GHz. The nominal phase noise at 1 MHz offset is -116.28 dBc/Hz, and the current consumption is 850 uA when 0.7 V VDD is supplied.



(a)



(b)

Figure 3. (a) Phase Noise Simulation Result of the proposed DCO (b) Direct Modulation Results after Gain Estimation

Table 1. Performance Summary

Process	CMOS 55nm	
Supply Voltage	0.7 V	
Oscillation Frequency	4.8 GHz	
1-bit Resolution	MSB	81.92 MHz
	LSB	5.12 MHz
	Fine	153.6 kHz
	DSM 5-bit	4.8 kHz
Total Frequency Range	4.571 GHz ~ 5.27 GHz	
Phase Noise@1MHz offset	-116.28 dBc/Hz	
Current Consumption	850 uA	

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