A Design of a Low Noise and Low Power Low Drop Out Regulator with Fast Settling Time Technique

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Abstract: This Paper presents a low noise and low power Low Drop Out regulator (LDO) with fast settling time technique. Using Low Pass Filter (LPF) at the output of Band Gap Reference (BGR) and using output shunt capacitor at the output of LDO are the most efficient ways of suppressing output noise. Its settling time, however, is extremely slow because of large resistance and capacitance. By adopting the proposed fast settling time technique, settling time becomes 6 times faster compared to the normal situation while maintaining outstanding output noise characteristics.

This circuit is designed in CMOS 55 nm process and the output noises are 300 nV/√Hz, 22 nV/√Hz, and 0.21 nV/√Hz at 10 kHz, 100 kHz, and 1 MHz, respectively. Settling time of LDO is 150 us and the output of the proposed LDO is 850 mV. The current consumption including BGR and LDO is 82 uA when the supply voltage is 1.2 V

Keywords—**Low Noise, Low Drop Out Regulator, Fast Settling Time**

1. Introduction

As supply voltage goes down under 1 V for low power consumption in various application such as Bluetooth Low Energy (BLE) application, output noise characteristic of Low Drop Out regulator (LDO) plays an important role in noise-sensitive analog blocks, especially Voltage Controlled Oscillator (VCO) in Phase Locked Loop (PLL) [1]. To satisfy the in-band phase noise specification of VCO, low output noise characteristic of LDO is really dominant. Moreover, noise of BGR, which provides a reference voltage of Error Amp of LDO, should be suppressed to reduce the output noise of LDO. Although using LPF at the output of BGR and using output shunt capacitor at the output of LDO are the most efficient way of suppressing output noise characteristic of LDO, its settling time is too slow because of the large resistance and capacitance of LPF and off-chip LDO output capacitance.

In this paper, by using LPF and output capacitor at the output of BGR and LDO, respectively, output noise of LDO can be suppressed. And by adopting the proposed fast settling technique, settling time becomes 10 times faster compared to the normal operation of LDO.

2. Architecture of the proposed LDO

Fig.1 shows the overall architecture of the proposed LDO. It consists of BGR, which generates the reference voltage of LDO, LPF, which is for suppressing output noise of LDO, fast settling structure, which is for achieving fast settling time of BGR and LDO, and LDO core, which generates supply voltage for analog circuits. When FAST_SET is high, which is the duration while BGR_PEN is high and LDO_PEN is low, at the initial sequence, BGR outputs the reference voltage through fast-settling transistor M0 so that BGR can charge the capacitor of LPF before LDO is turn on while maintaining stable output reference voltage.

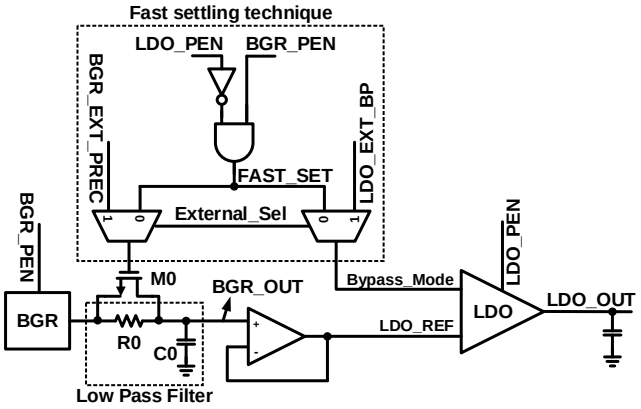

Figure 1. Overall Architecture of the proposed LDO

Fig.2 shows the detail schematic of LDO. As can be seen from the Fig.1 and Fig.2, when FAST_SET is high, bypass mode of LDO becomes high so that pass transistor M14 of LDO is turn on and supply voltage of LDO directly becomes the output of LDO with voltage drop of M14.

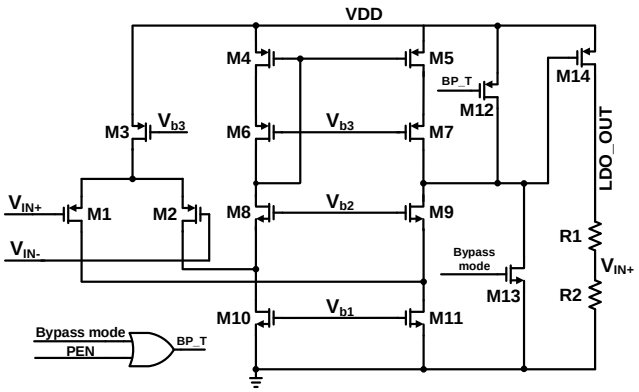

Figure 2. Detail Schematic of the proposed LDO Core

Output noise specification of LDO, especially for VCO supply voltage, can be determined by the equation below

$$L_{TOTAL} = 10log\left[10^{\frac{L_{VCO}}{10}} + 10^{\frac{L_{LDO}}{10}}\right] \quad \ldots (1)$$

$$V_{LDO}(f) = 10^{\frac{L_{LDO}}{20}} \times \frac{\sqrt{2}\times f}{K_{push}} \quad \ldots (2)$$

, where L_{TOTAL} denotes the overall LDO output noise, L_{VCO} denotes the voltage noise spectral density of the LDO at a given frequency offset in V/√Hz, L_{LDO} denotes the noise contribution from the regulator to the VCO phase noise in dBc/Hz, K_{push} denotes the VCO pushing figure in Hz/V, and f denotes the frequency offset in Hz [2]. For example, in BLE application, phase noise specification at 100 kHz offset is -80 dBc/Hz and assuming K_{push} of VCO is 80 MHz/V, then LDO output noise should be under 88 nV/√Hz.

3. Simulation Results

Fig.3(a) shows the output noise results of the proposed LDO. As can be seen from the results, output noise are 300 nV/√Hz, 22 nV/√Hz, and 0.21 nV/√Hz at 10 kHz, 100 kHz, and 1 MHz, respectively.

Fig.3(b) shows the transient results when External_Sel is low so that internal fast settling mode can operates. Output voltage of BGR, BGR_OUT, is 463 mV and the output voltage of LDO, LDO_OUT, is 850 mV. As can be seen from the results, settling time of LDO is about 150 us after LDO_PEN is high, which is about 6 times faster than normal mode.

This circuit is designed in CMOS 55 nm process and the current consumption is 82 uA including BGR and LDO when the supply voltage of 1.2 V is supplied from the battery. Table 1 shows the overall performance summary.

Table 1. Performance Summary

Process	CMOS 55 nm
Supply Voltage	1.2 V
Output Noise	300 nV/√Hz @10 kHz 22 nV/√Hz @100 kHz 0.21 nV/√Hz @1 MHz
Output Voltage of LDO	850 mV
Current Consumption	82 uA (including BGR & LDO)

4. Conclusion

This paper presents a low noise and low power LDO with fast settling time technique. To achieve low output noise specification and fast settling time at the same time, LPF and fast settling time technique are used. For the fast settling, the output capacitors of BGR and LDO are pre-charged before LDO starts to operate.

This circuit is designed in CMOS 55 nm process and the output noises are 300 nV/√Hz, 22 nV/√Hz, and 0.21 nV/√Hz at 10 kHz, 100 kHz, and 1 MHz, respectively. Settling time of LDO is 150 us which is 6 times faster than normal mode. The current consumption including BGR and LDO is 82 uA and the output voltage of LDO is 850 mV when the supply voltage is 1.2 V.

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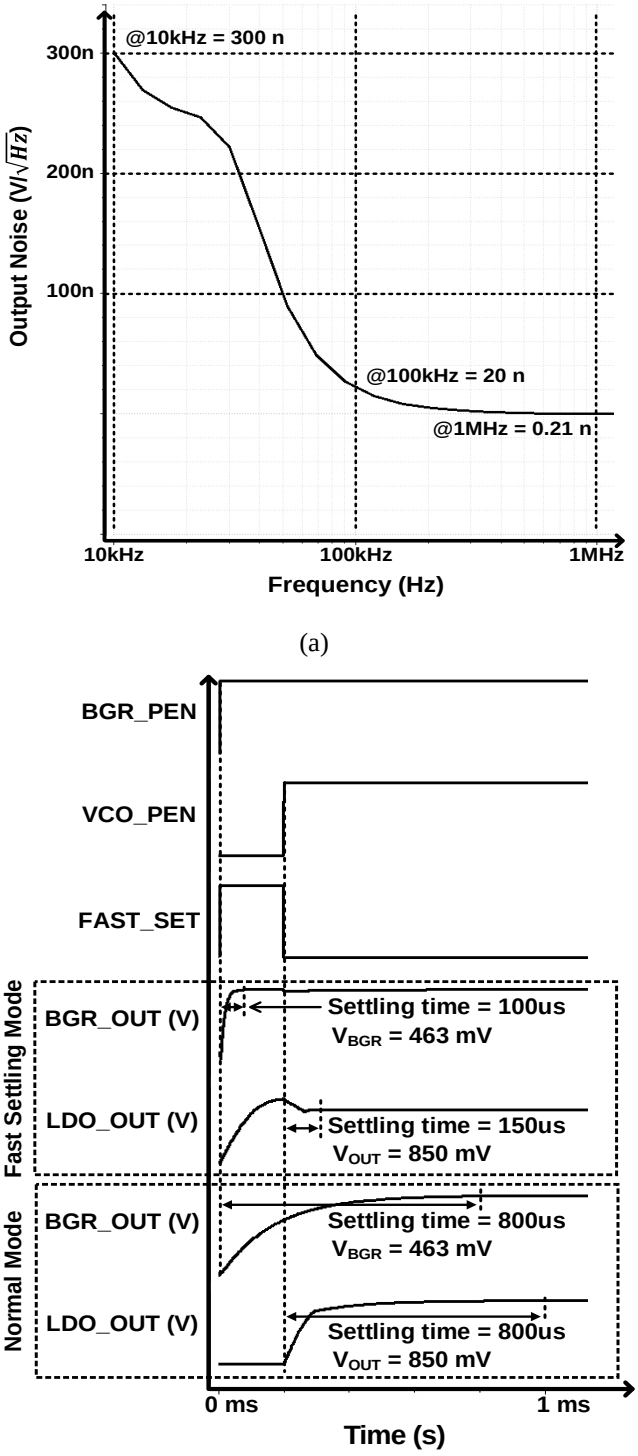

Figure 3. (a) LDO output noise characteristics (b) Transient Simulation Results of the proposed LDO

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