Self-Terminated Read for Reduced Read Disturbance and Power Consumption in Large Cross-Point ReRAM Arrays

Hyun-Seok Kang and Kee-Won Kwon
College of Information and Communication Engineering, Sungkyunkwan University, Suwon, Korea
keewkwon@skku.edu

Abstract: This paper presents self-terminated read scheme for improving read disturbance and reduction of power consumption in large cross-point ReRAM arrays. The residual read stress prolongs after the decision is made resulting in problems of read disturbance and undesirable power consumption. Startable time for sensing can be also reduced by 13.76ns. Elimination of unneccessary read stress cuts the total stress by 80% saving the read power by 40.63% in 1-Mb cross-point ReRAM array. The read disturbance is improved about 10 times compared to conventional scheme.

1. Introduction

Resistive random access memory (ReRAM) has many advantages such as it fast read, write speed, large resistance-ratio, compatibility with the present technology, scalability and simple structure. [1] So, it is considered to be promising nonvolatile memory for next generation and it is, especially, realizable to organize 3D stackable IC design in large ReRAM arrays.

However, using transistor as selector can't be possible in 3D stack ReRAM array because of fabrication problem. [2] Therefore, unselected cells in ReRAM array should be biased as ground to resolve sneak current issue and ensure read reliability. In this case, problems of power consumption and read disturbance enormously increase as ReRAM array size increases.

If the read stress is terminated, as soon as finishing read operation, the problem of power consumption and read disturbance will be remarkably improved. The design method of self-terminated read scheme (STRS) will be proposed in this paper.

2. Conventional read sheme and read disturbance with T.D.D.B

ReRAM is called resistive swithching memory because it stores the data in a form of conductivity of memory elements. The level of resistance switches between the high resistance 'reset' state (HRS) and the low resistance 'set' state (LRS) by applying bias voltage between top electrode (TE) and bottom electrode (BE).

Figure 1 shows a mechanism of set/reset operation respectively. Depending on the proper set/reset voltage between TE and BE, set and reset operation is generated and the mechanism of set operation is defferent from reset operation in Figure 1. [3]

Figure 2 represents that the average set and reset voltage is about 1.3V and -1.8V from mesurement results, respectively. Therefore, it is resonable to fix the initial read voltage to 1V from measurement results of figure 2 in conventional paper and this paper.

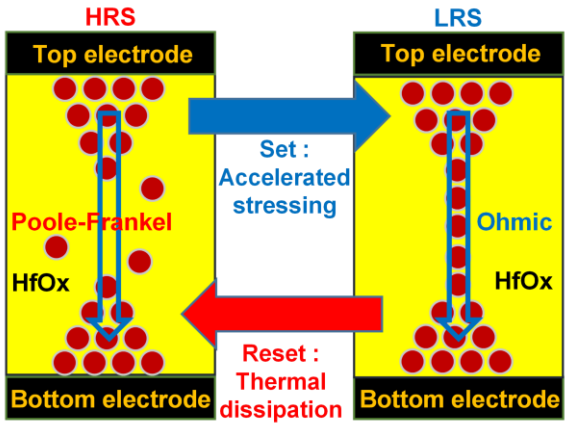

Figure 1. Expected mechanism of HfOx-based ReRAM cell.

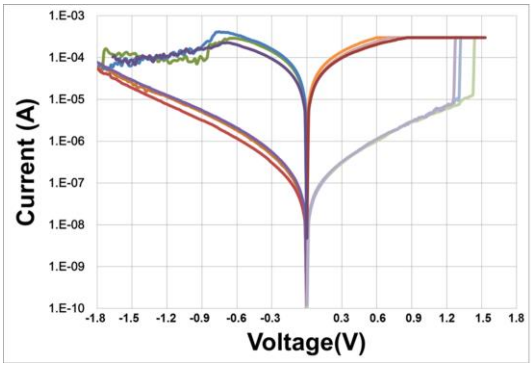

Figure 2. I-V curves of ReRAM arrays from measurement.

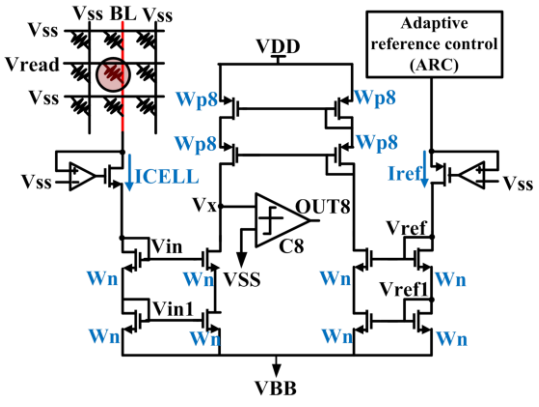

Figure 3. Conventional read scheme in ref [5].

Figure 3 and Figure 4 show conventional read circuit and its timing diagrams, respectively. In Figure 3, when VREAD results in ICELL, Vin is developed to specific level by LRS or HRS cell state and gate voltage of Wp8 is fixed by Iref and Vref that are properly decided by ARC. [4]

And then, Vx can be decided to VDD or VBB by comparing strength of pmos (Wp8) and nmos (Wn). In this operation, Vin and Vx are to be steady-state within 10ns and 20ns empirically. That's why VREAD is enabled and after about 20ns, FETCH signal is asserted to C8 for read operation. [5] In this case, however, read stress is not stopped, as soon as finishing read operation. In other words, unwanted redundant VREAD stress is applied to the cells for about 20ns after FETCH signal is asserted.

Time-dependent dielecetric breakdown (TDDB) measurements have been widely reported in paper using concept of Weibull shape factor.

$$F(T_{BD}) = 1 - \exp\left(-\frac{T_{BD}}{\alpha}\right)^{\beta} \quad (1)$$

$$\text{Unreliability } (W) = \ln\left[-\ln(1 - F(T_{BD}))\right] \quad (2)$$

In Eq. (1), F is the cumulative failure probability, which is an extrem-value distribution. α is the caracteristic time-to-breakdown at the failure percentage of 63% and β is the Weibull shape facter, also called as Weibull slope. In Eq. (2), unreliability (W) of dielectric such as oxide has been plotted in a form of nomarized T_{BD} that shows straight line with slope β. Because this parameters and equations are related to reliability, it is possible to expect how much the read disturbance improves. In figure 5, α called T_{63} of oxide is increased as gate voltage rises and reliability is degraded by time-to-breakdown (T_{BD}) and figure 6 shows that unreliability of HfO2 is proportional to ln(T_{BD}). [6], [7]

Therefore, if it is possible to reduce redundant read stress time or the level of Vread, read reliablility and the number of read access can be improved. In this paper, the initial Vread is fixed to 1V. Therefore, with STRS, Vread stress time related to T_{BD} will be reduced and it is eventually, predictable to not only reduce power consumpiton but also enhance read disturbance and reliability in large cross-point ReRAM arrays.

3. Self-terminated read scheme (STRS)

Figure 7 shows the full scheme of STRS proposed in this paper. The timing diagrams of STRS, as depicted in figure 8, are as follows. Compared to conventional scheme, STRS includes additional 5 blocks.

At first, EN is enabled by READ_EN with one AND gate delay because signal Q is set to high initially. ENB switch turns off initialization circuits such as figure 7. (d), (e), then Vin and Vx that was set to Vref and Vss, respectively, starts to rise or fall by cell state. It is not possible to do read operation exactly without initialization of Vx and Vin, because Vin is set to VBB at first and Vx always falls regardless of cell state.

When Vx touches Vref_LRS/HRS and after 1 comparator and 1 OR gate delay, TERM_F is to be high. Because the D-F/F in figure 7 operates using TERM_F signal as clock signal, after 1 D-F/F delay, Q signal is to be VBB in figure 8. (1). EN is disabled by Q signal in 1 AND gate delay. As soon as read stress termination by ENB signal, D-F/F starts to read monitoring level of Vx by ENB and saves a data of cell state until next read operation in

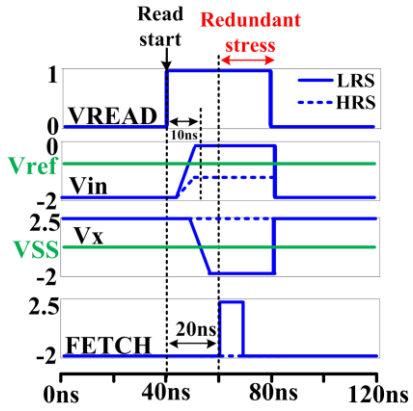

Figure 4. Timing diagrams during normal read mode in Figure 3.

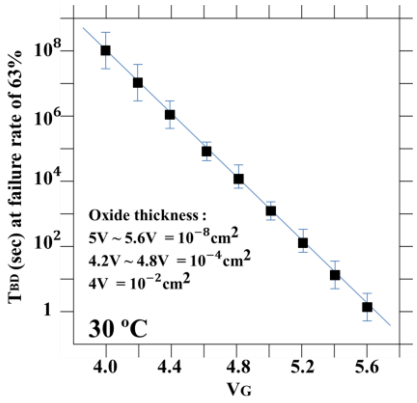

Figure 5. Measured T_{BD} distribution at failure rate of 63% for gate voltages from 4V to 5.6V.

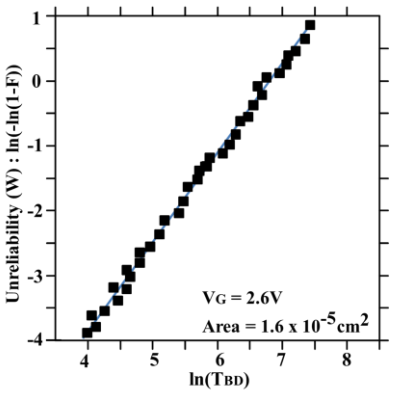

Figure 6. Weibull destribution of HfO_2. Unreliablilty increases as T_{BD} is increased.

figure 7. (e) and figure 8. (2). Then, Vx and Vin returns to Vss and Vref, respectively, almost simultaneously by initialization circuits. Finally, TERM_F is disabled and Q signal returns to VDD by READ_EN.

4. Simulation results

Figure 9 represents monte-carlo simulation result used 350nm CMOS technology. Left plain shows STRS operation in HRS cell state and the oppsite one appears in

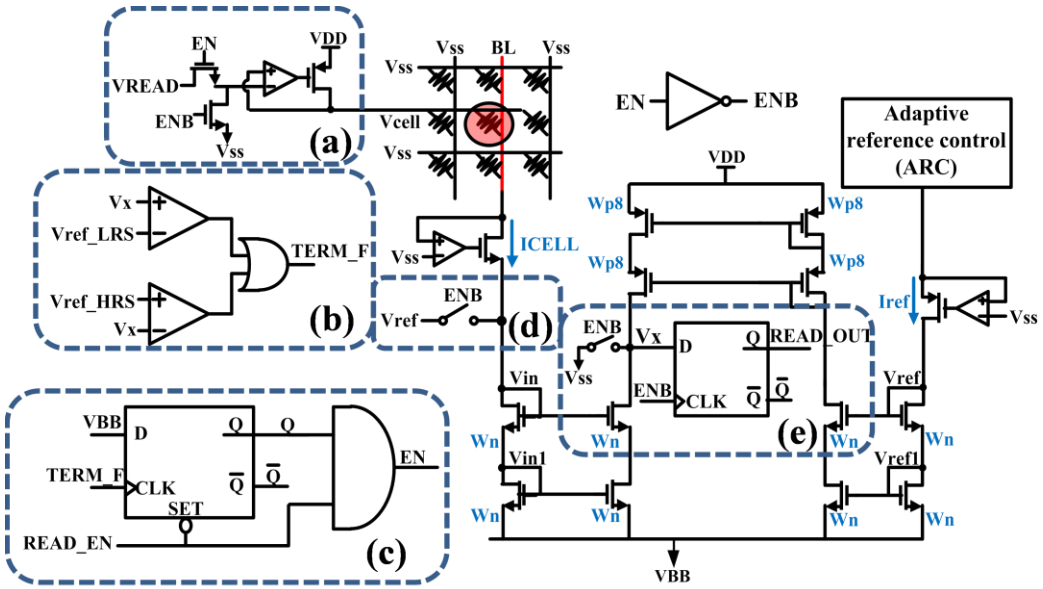

Figure 7. Whole circuits of STRS. (a) VREAD is terminated by EN signal. (b) TERM_F signal generator. (c) EN signal generator. (d) Vin is forced as Vref with switch. (e) Read data is saved by D- F/F for 1 READ_EN cycle.

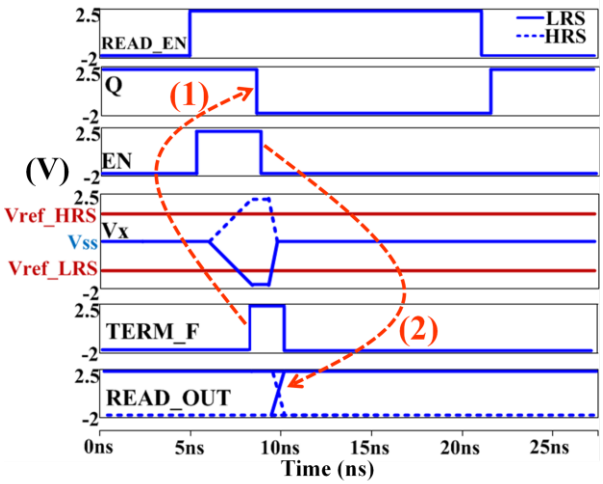

Figure 8. Timing diagrams applied STRS.

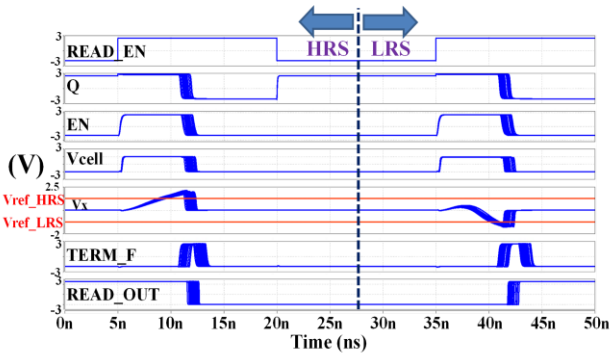

Figure 9. Monte-carlo simulation of STRS.

LRS cell state based on 27ns. As presented in Figure 7. (a), Vcell is terminated by EN switch signal. Vcell pulse time can be reduced from about 40ns to 8ns by 80% for both of LRS and HRS. As READ_OUT signal represents the cell

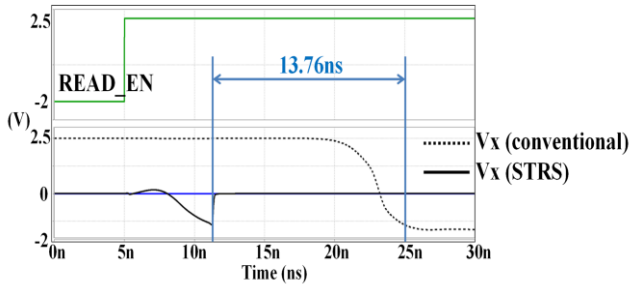

Figure 10. Startable time for sensing can be reduced by 13.76ns due to initialization of Vx and Vin.

state, the data can be maintained for 1 READ_EN cycle. EN signal is made from READ_EN, that's why D-F/F synchronized ENB signal in figure 7. (e) operates only once every one READ_EN cycle.

Figure 10 shows why FETCH should not be asserted eariler than 20ns after READ_EN signal is enabled in conventional read scheme. Compared to conventional scheme, STRS initializes Vin and Vx to middle level such as Vref, Vss respectively, that's why startable time for sensing can be reduced by 13.76ns. As a result, STRS doesn't need to last read stress by 20ns and read pulse time can be remarkably cut.

Figure 11 represents the quantity of reduction of power consumption in all 1-Mb LRS ReRAM arrays. Although the unselected cells should be biased to ground not floating conditions for retaining read reliability because of sneak current issue, read power consumption is reduced up to 40.63% with STRS. It is expected that the effect of reduction of power consumption is increased as ReRAM array size grows more and more.

The number of read access increases about 10 times cycling from 10^5 to 10^6 with STRS in Figure 12. As a result, STRS can improve read disturbance and retain wide read margin.

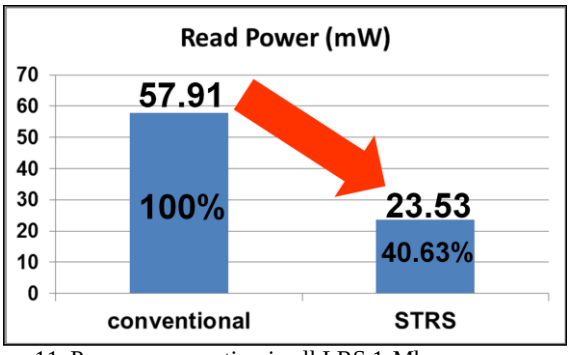

Figure 11. Power consumption in all LRS 1-Mb arrays.

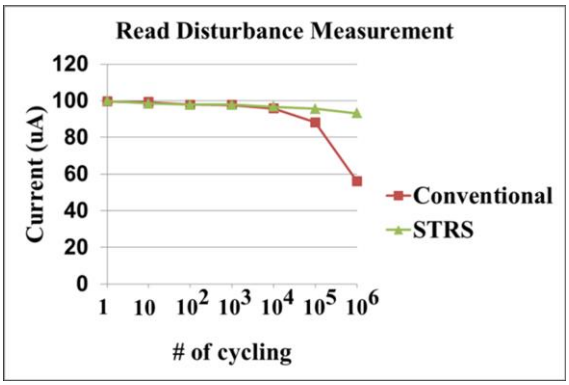

Figure 12. Improvement of read disturbance in read current of LRS with STRS.

5. Conclusion

This paper suggested an effective method for improving read disturbance and reducing power consumption with STRS. Even though it needs to additional area, the STRS helps to cut total read stress by 80% and reduce startable time for sensing by 13.76ns, so that power consumption could be decreased by 40.63% in all LRS 1-Mb ReRAM arrays. The read disturbance is improved about 10 times compared to conventional scheme.

References

[1] H. Akinaga, et al., "Resistive Random Access Memory(ReRAM) Based on Metal Oxides," *Proceedings of the IEEE*, 98, pp.2237-2251, 2010

[2] H. D. Lee, et al., "Integration of 4F2 Selector-less Crossbar Array 2Mb ReRAM Based on Transition Metal Oxides for High Density Memory Applications," *Symp. VLSI Tech*, pp. 151-152, 2012

[3] F. T. Chen, et al., "Size dependence of TiN/HfO2/Ti MIM ReRAM resistance states: model and experimental results," *Current Appl. Phys.*, vol.10, no.1, pp. 75-78, Jan 2010

[4] J.-K. Park, S.-Y. Kim, J.-M. Baek, D.-J. Seo, J.-H. Chun, and K.-W. Kwon, "Analysis of resistance variations and variance-aware read circuit for cross-point ReRAM," in *Proc. IMW*, 2013, pp. 112–115.

[5] S.-Y. Kim, J.-M. Baek, D.-J. Seo, J.-K. Park, J.-H. Chun, and K.-W. Kwon, "Power-efficient fast write and hidden refresh of reram using an adc-based sense amplifier," *IEEE Trans. Circuits Syst.–II:Express Briefs*, vol. 60, no. 11, pp. 776–780, 2013.

[6] Y. H. Kim, K. Onishi, C. S. Kang, H.-J. Cho, R. Nieh, S. Gopalan, R. Choi, J. Han, S. Krishnan, and J. C. Lee, "Area dependence of TDDB characteristics for HfO gate dielectrics," *IEEE Electron Device Lett.*, vol. 23, pp. 594–596, Oct. 2002.

[7] E. Y. Wu, J. Sune, and W. Lai, "On the Weibull shape factor of intrinsic breakdown of dielectric films and its accurate experimental determination. Part II: Experimental results and the effects of stress conditions," *IEEE Trans. Electron Devices*, vol. 49, no. 12, pp. 2141–2150, Dec. 2002.