A Self-reference Sensing to Compensate Data Pattern Dependent Leakage Current in the Cross-point ReRAM Array

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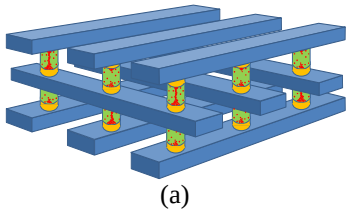
Abstract: This paper presents a self-reference sensing which could compensate data pattern dependent leakage current that acts as a noise in cross-point ReRAM array. There has not been such a clear solution for the leakage current issue without using selector devices, because the leakage current variation is random and wider than the difference of the cell states. Proposed self-reference sensing uses analog subtractor to compensate the leakage current which varies with unpredictable data pattern. This compensation leads us to get a uniform and enough (over 30mV) sensing margin superior to 2mV of the conventional one in the worst case of data pattern.

1. Introduction

NAND Flash memory edged out Hard Disk Drive (HDD) in the storage class memory (SCM) lately, because NAND Flash has far higher read/write speed, longer endurance, and more reliability than HDD. Unfortunately, the future of NAND Flash is not that clear because of its capacity issue. As the process shrinks the reliability of NAND Flash decreases dramatically, because the number of manageable electrons in the floating gate reduces. There are several candidates, which could be proper for the next generation SCM, and Resistive Random Access Memory (ReRAM) is one of those candidates.

ReRAM is known for its high endurance, low switching power, fast read/write speed, and high on/off ratio [1, 2]. The cross-point ReRAM array has very simple and stackable structure. As shown in Figure. 1. (a), the cell itself can be located between the metal layers like a via. Therefore, we can have more area-efficient memory applications. ReRAM cell structure is illustrated in Figure. 1. (b). The high-k dielectric materials, such as HfOx and TaOx, are generally used as memory element in the ReRAM, and its state is initially High Resistance State (HRS). When the voltage across the memory element reaches set voltage, oxygen vacancies in the memory element are gathered to form a conducting filament (CF), then current can flow through this CF. This state is called Low Resistance State (LRS). As we force the reverse bias across this LRS cell to the reset voltage, oxygen vacancies are scattered from the CF. Then the state of the cell goes back to HRS. We consider the HRS as data '0' and the LRS as data '1'.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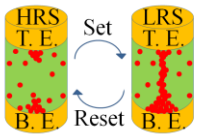

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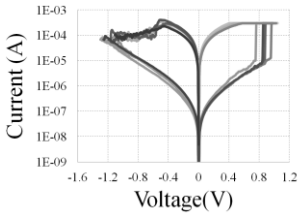
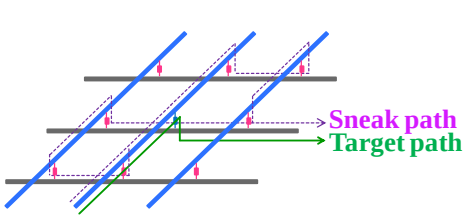


(c)

Figure. 1. (a) Cross-point array, (b) Cell structure, and (c) I-V curve of ReRAM



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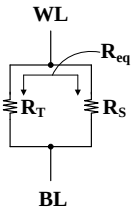

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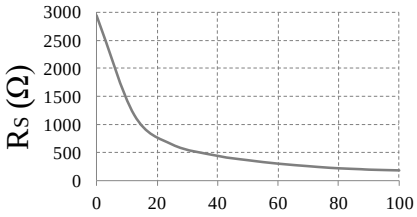

(c)

Figure. 2. (a) Sneak paths (b) Equivalent circuit of cross-point ReRAM array (c) Sneak resistance variation depending on LRS portion in the array

2. Leakage Current and Self-reference Sensing

2. 1 Leakage current in cross-point ReRAM array

Leakage current is the primary issue of cross-point ReRAM array [3]. There could be many possible bypasses in the array like in Figure. 2. (a), due to the simplicity of cross-point structure itself. The leakage current flows through these sneak paths and degrades the sensing signal. We can see this leakage current as a noise similar to the case of RF module depicted as Figure. 3. In RF module, the eye diagram is distorted by channel noise, and we should equalize it before we handle the signal well. Likewise, the leakage current has to be compensated properly.

The leakage current is mainly affected by two factors. One is data pattern (or LRS portion in array), which we could not predict. As the data pattern is generated, equivalent sneak resistance (R_S) decreases as described in figure. 2. (c). The other factor is the location of target cell

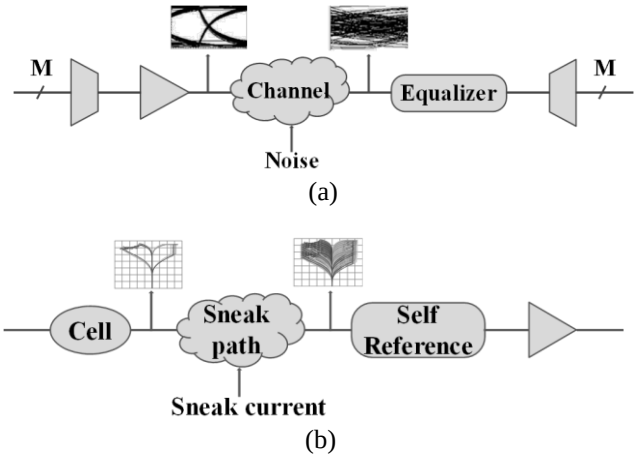

Figure. 3. Signal characteristic in (a) RF module and (b) cross-point ReRAM array

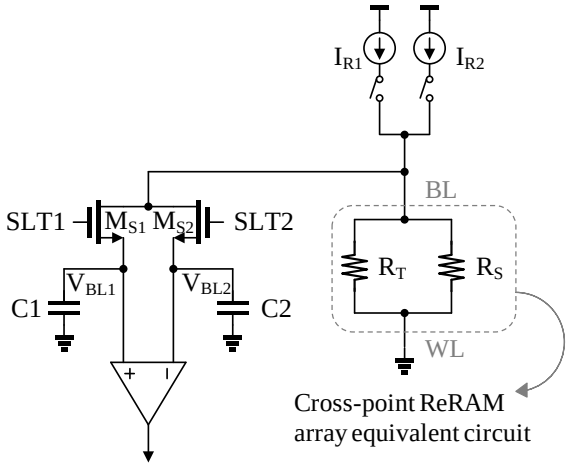

Figure. 4. Conventional self-reference sensing adapted in cross-point ReRAM array

because the sneak paths change depending on the target location, even though the data pattern is same. If the variation depending on the cell position is larger than the difference between HRS and LRS of the cell, negative SNR can occur and we cannot distinguish the signal from noise successfully with simple voltage or current sensing widely used. To sense the desired data correctly, we adapted self-reference sensing [4].

2. 2 Self-reference sensing

Figure. 4 is the schematic of conventional self-reference sense amplifier [4]. The circuit consists of two current sources (I_{R1} and I_{R2}), two switches (M_{S1} and M_{S2}) controlled by 'SLT1' and 'SLT2' signals, two capacitors (C1 and C2), and a voltage comparator. The operations of this circuit are followed:

(1) First read: WL to the ground and I_{R1} flows through the BL. Successive BL voltage (V_{BL1}) is stored in the C1 capacitor while the M_{S1} switch is on and M_{S2} switch is off.

(2) Reset: Reset the target cell to HRS regardless of the previous state, while both switches are off.

(3) Second read: I_{R2} which is a bit smaller than I_{R1} flows through the BL and successive BL voltage V_{BL2} is stored in the C2 capacitor while M_{S2} switch is on and M_{S1} switch is off. The amount of difference between I_{R2} and I_{R1} should be chosen to satisfy the following condition:

$$V_{BL1\_L} < V_{BL2} < V_{BL1\_H}$$

V_{BL2} play a role of reference voltage and consecutive output would be offered by comparator.

(4) Write back: Restore the readout data.

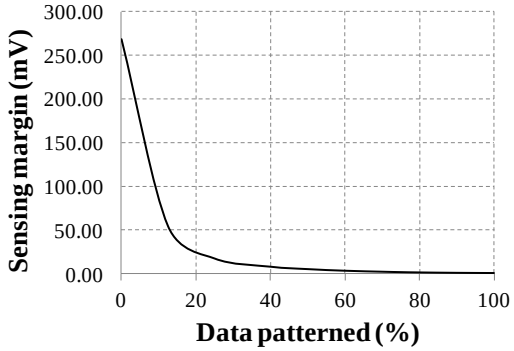

Figure. 5. Sensing margin in conventional self-reference sensing (I_{R1} = 300μA, R_L = 5.3kΩ)

The conventional self-reference sensing uses read currents to generate voltage signals to sense. In the case of cross-point ReRAM array, this read current leaks through sneak paths and leaks more as sneak resistance becomes smaller. After all, the sensing margin shrinks to read fail the data. We can simplify the cross-point array into simple equivalent circuit like in figure. 2. (b). As the data pattern generates, equivalent sneak resistance (R_S) decreases shown as figure. 2. (c). If we denote the ratio of ReRAM cell is α (R_H = αR_L), sensing margin (SM) can be calculated as follows:

$$V_L = I_{read} R_{eqL}, \quad V_H = I_{read} R_{eqH}$$

$$SM = I_{read} R_{eqL} - I_{read} R_{eqH} = I_{read} \Delta R_{eq}$$

$$R_{eqL} = \frac{R_L}{R_L + R_S}, \quad R_{eqH} = \frac{R_H}{R_H + R_S}$$

$$\therefore \Delta R_{eq} = \frac{(\alpha - 1) R_L}{\alpha \left(\frac{R_L}{R_S}\right)^2 + (\alpha + 1)\left(\frac{R_L}{R_S}\right) + 1}$$

$$\therefore SM = I_{read} \Delta R_{eq} = \frac{(\alpha - 1) I_{read} R_L}{\alpha \left(\frac{R_L}{R_S}\right)^2 + (\alpha + 1)\left(\frac{R_L}{R_S}\right) + 1}$$

We could verify that the sensing margin is dependent on R_S square, while other parameters are constant. Figure. 5 shows relation between sensing margin and data pattern which determine R_S.

3. Proposed Self-reference Sensing Circuit

3. 1 Concept of proposed circuit

The conventional way could resolve the negative SNR problem. However it uses the read current which could leak through sneak paths. This leak brings out degradation of sensing margin. To get a uniform sensing margin independent of data pattern, we should use a read voltage

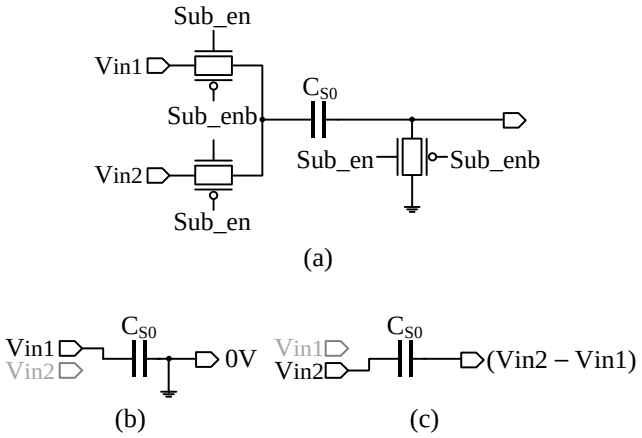

Figure. 6. (a) Analog subtractor and its operations (b) Sub_en = VDD (c) Sub_en = VSS

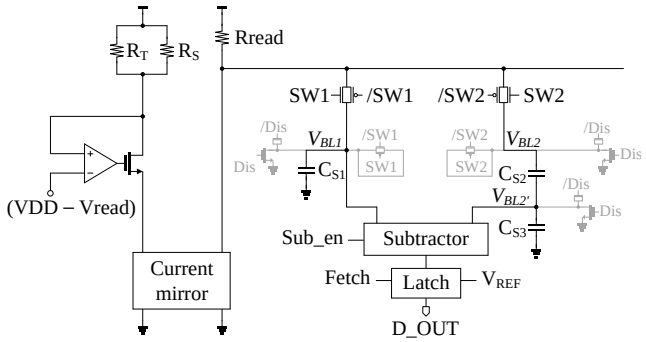

Figure. 7. Full schematic of proposed circuit

instead. In that case, we can get a uniform signal difference between HRS and LRS.

Firstly, we bias the read voltage across the selected WL and BL while other WLs and BLs are uncharged. Then, the following read current would come out and we should store this signal until the second read signal reaches. We bring into play a resistance to convert current into voltage signal (R_{read}). After that we can store the signal in the capacitor and compare them like conventional way with no degradation of sensing margin. The full schematic of proposed circuit is illustrated in Figure. 7.

3. 2 Leakage current compensation

Each signal (V_{BL1} and V_{BL2}) has a noise which contains the information of leakage current, and their quantities are equal. Therefore, a pure signal can be obtained by subtracting them. We use analog subtractor composed of three switches controlled by 'Sub_en' signal and a capacitor (C_{S0}) as depicted in Figure. 6. When 'Sub_en' is VDD, the left side of CS0 is biased as Vin1 and the right side to ground. After 'Sub_en' becomes VSS, voltage of the right side of C_{S0} increases the amount of the difference between Vin2 and Vin1 because the charge stored in C_{S0} must be maintained. We could find out that the sensing margin of proposed way is independent of R_S in the following equations, whereas conventional one is not.

$$I_L = \frac{V_{read}}{R_{eqL}}, \quad I_H = \frac{V_{read}}{R_{eqH}}$$

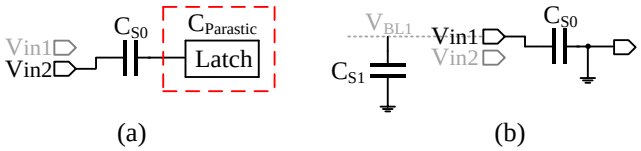

Figure. 8. Charge distribution between (a) C_{S0} and $C_{Parastic}$ (b) C_{S1} and C_{S0}

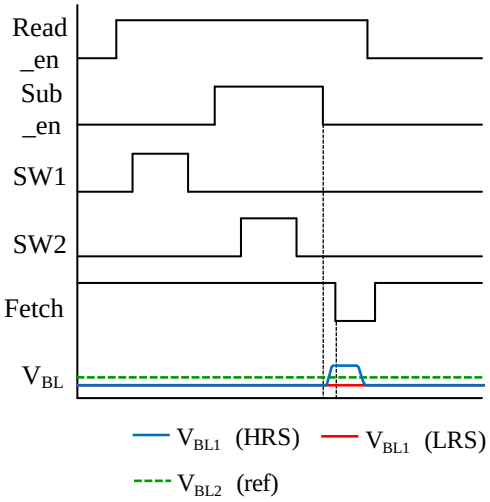

Figure. 9. Timing diagram of proposed circuit

$$\Delta I = \frac{V_{read}}{R_{eqL}} - \frac{V_{read}}{R_{eqL}} = V_{read}\left\{(R_{eqL})^{-1} - (R_{eqH})^{-1}\right\}$$

$$= V_{read}\,\Delta(R_{eq})^{-1}$$

$$(R_{eqL})^{-1} = R_L{}^{-1} + R_S{}^{-1}, \quad (R_{eqH})^{-1} = \alpha R_L{}^{-1} + R_S{}^{-1}$$

$$\therefore \Delta(R_{eq})^{-1} = \left(\frac{\alpha}{(\alpha-1)}R_L\right)^{-1}$$

$$\Delta I = V_{read}\,\Delta(R_{eq})^{-1} = V_{read}\left(\frac{\alpha}{(\alpha-1)}R_L\right)^{-1}$$

$$\therefore SM = R_{read}\,\Delta I = R_{read}\,V_{read}\left(\frac{\alpha}{(\alpha-1)}R_L\right)^{-1}$$

3. 3 Charge sharing issue

We use some capacitors to deal with voltage signals in the proposed circuit, and there are two points where the critical charge sharing occurs as shown in Figure. 8. The C_{S0} of subtractor is attached to a transistor gate of the latch, and its capacitance shares the charge with C_{S0}. To minimize the loss of signal, we take the size of C_{S0} large enough compared to $C_{Parastic}$. This relatively large capacitor C_{S0} is connected to C_{S1} when 'Sub_en' signal is high. In that phase, the charge induced by V_{BL1} and stored in C_{S1} is shared with C_{S0}. The size of C_{S1} is four times larger than C_{S0} so that the loss of voltage signal would be 20% by charge sharing. Vin2 of subtractor should be matched, so we put two capacitors on the right branch. The size of C_{S2} is set to be the same as C_{S1}, and C_{S3} a C_{S0}

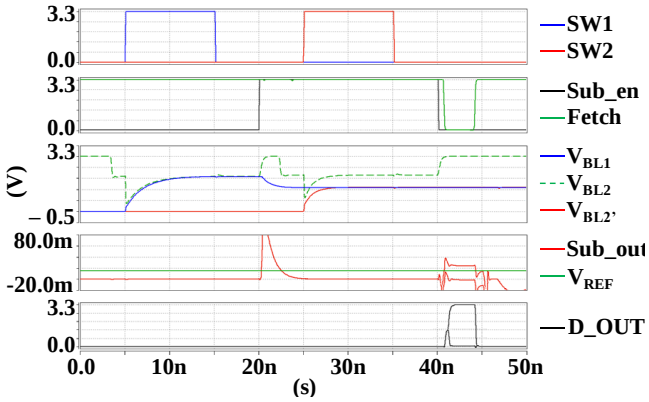

Figure. 10. Simulation result of data pattern = 50%

Table. 1. Parameters used in the proposed circuit

Parameter	Description	Value
R_L	LRS resistance	5.3 kΩ
α	Ratio between HRS and LRS	13.2
R_{read}	Read resistance	700 Ω
V_{read}	Read voltage	0.4 V
C_{S0}	Capacitor used in Subtractor	0.5pF
C_{S1}	To store V_{BL1} signal	2pF
C_{S2}	To store V_{BL2} signal	2pF
C_{S3}	To store V_{BL2} signal	0.5pF

3. 4 Peripheral block of proposed circuit

The charges remained in C_{S0} ~ C_{S3} should be clear after each read operation is over. The three NMOS transistors controlled by 'Dis' signal discharge these capacitors when the read operation is done. These transistors plus two pass transistors controlled by 'SW1' and 'SW2' signals could induce channel charge injection problem on their driving nodes when they are off. To compensate these channel charges, we should put dummy switches controlled by reverse signal of the reference signal. The size of them should be half of the original switches, because sources and drains of the dummy switches are tied. These peripheral components are drawn in gray color in Figure. 7.

4. Simulation results

Parameters necessary for the proposed circuit are described in Table. 1. We evaluate performance with HSPICE simulation tool based on the magna 350nm process design using virtuoso. Proposed sensing could read successfully independent of data pattern while conventional one fails when the data pattern goes above about 50%. One example of simulation when data pattern is 50% is shown in Figure. 10. The overall sensing margin tendency is depicted in Figure. 11. The solid lines represent simulation results. Proposed way guarantees over 30mV margin regardless of data pattern, whereas the margin of conventional way decreases under 20mV when data pattern becomes more than 25%, and it degrades below 5mV in excess of 55% data pattern. Table. 2 has information about the post-layout simulation on each corner condition. The minimum sensing margin is 26.87mV on FSF corner, and the maximum margin is 37.88mV on SFS corner.

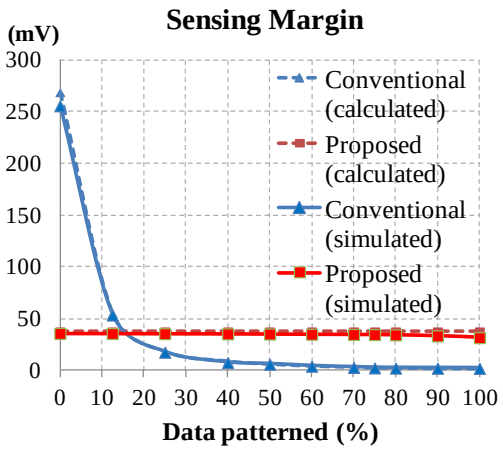

Figure. 11. Sensing margin comparison

Table. 2. Average sensing margins of each corner shift on post-layout simulation

Corner	Sensing margin	Corner	Sensing margin
FFF	28.19 mV	SSS	36.64 mV
FST	34.19 mV	SFT	35.34 mV
FSS	36.02 mV	SFS	37.88 mV
FSF	26.87 mV	SFF	28.59 mV
TTT	34.76 mV		

5. Conclusion

We propose a revised self-reference sensing suitable for compensating arbitrary leakage current in cross-point ReRAM array. At last, we success to get a uniform sensing margin no matter how much data pattern is generated. Without selector devices, this sensing technique is the only and the best way immune to random data pattern. However, that there are two write processes during one read operation causes some operational issues. If sudden power off happens after 'reset' process and before 'write back' step, the data can evaporate and there is no way to find out what the real data was after the power returns. To prevent this unexpected power loss, we should use a large power capacitance as a role of spare battery that could holds until the 'write back' operation is done. Longer read latency ($\geq t_{write} + 2t_{read}$) issue could be dealt with parallel sensing at the same time, which needs further researches in the cross-point array environment. Read endurance is also significantly damaged because of the two write processes. However, this issue could be ignored because the decreased read endurance of ReRAM still fall higher than that of NAND Flash memory currently used well.

References

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