All-Digital and Low-Power Reference Clock Generator for Biotelemetry Applications

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Abstract: In this paper, an all-digital and low-power reference clock generator with cell-based design for biotelemetry applications is presented. The proposed clock generator employs a cascade-stage structure to achieve high resolution and wide range at the same time. Besides, based on the proposed Schmitt-trigger-based delay cell (STDC), the proposed clock generator not only can provide high resolution, but also can generate low frequency clock signal with low power consumption and low circuit complexity as compared with conventional approaches. Simulation results show that the operation frequency range is from 7.9MHz to 120.8MHz, and the power consumption can be improved to 54μW (@7.9MHz) with 10.5ps resolution. In addition, the proposed clock generator can be implemented with standard cells, making it easily portable to different processes and very suitable for biomedical System-on-Chip (SoC) applications.

Keywords-- **WBAN, DCO, Clock Generator**

1. Introduction

As the wireless communication and integrated circuit (IC) technology develop rapidly, the medical services extend from the closed in-hospital systems to any open roaming spaces. Through the wireless communication, the physiological information of patient that provided by the wearable or implantable devices in the body can send to the hospital for healthcare and health monitoring immediately. Figure 1 illustrates the concept of wireless healthcare and health monitoring system. The physiological signals transmits to the personal server, such as a smart phone, by wireless body area network (WBAN), and then delivers it to the hospital or medical server by wireless networking [1]. Recently, there is a large of demand in biotelemetry application; the standard of WBAN was defined in [2].

A typical WBAN system is shown in Figure 2. Generally, a WBAN system consists of a multiple of wireless sensor nodes (WSNs) and a central processing node (CPN). According to the requirements of the healthcare and health monitoring, there are several important design considerations in WBAN system [3]: First, the WSN should have an ultra-low power operation [3]. Second, as the medical devices implanted into body, the size should be as small as possible for comfortable purposes. In addition, the circuit complexity of the implanted chip should be reduced to shrink the overall device area. Finally, the WBAN is required to provide reliable signal transmission for accurate healthcare and monitoring. Thus, especially in WSN, the quality of system clock source is very important.

The WSN design usually utilizes the power management with sleep/wakeup scheme to reduce the redundant power consumption [3]. However, the system still consumes power when it moves from sleep to wakeup status. Besides, long settling time degrades the overall system performance. Thus, how to reduce the settling time of WSN is an important design consideration. Traditionally, the reference clock of WSN is provided by a quartz crystal. The frequency synthesizer, such as a phase-locked loop (PLL), receives the reference clock from an off-chip crystal, and then generates the system clock signal with the desired frequency for WSN system. Generally, the output clock frequency range of a quartz crystal is from thousands Hz to several MHz. Based on these frequency range, the settling time of PLL is 100μs even 1ms [4], [5]. It can increase reference clock frequency to reduce the settling time of PLL to meet the system requirements [4]. However, as the reference clock frequency increases, it not only increases the power consumption of PLL, but also reduces the input noise immunity. In addition to the settling time issue, the size of quartz crystal is too large and hard to integrate into SoC, it is not suitable for the WSN in WBAN applications.

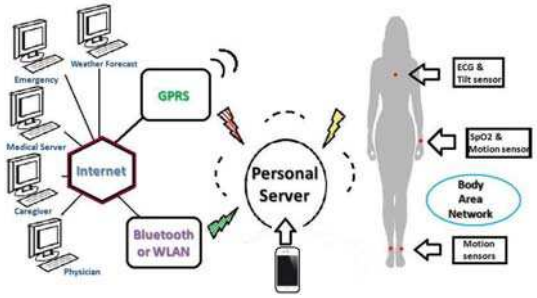

Figure 1. Concept of wireless healthcare and health monitoring system.

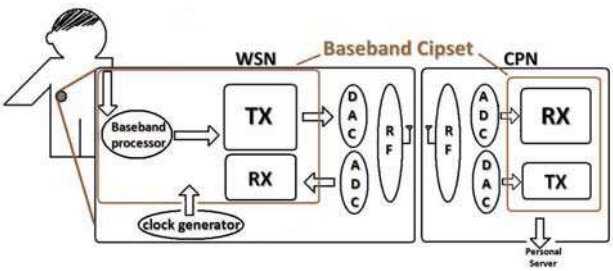

Figure 2. Architecture of WBAN system.

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Recently, a digitally controlled oscillator (DCO) as an all-digital reference clock generator for WBAN applications has been proposed [3], [6]-[8].The output clock frequency of DCO is controlled by the digital control code. If a DCO replaces a quartz crystal as a reference clock generator, it can integrate into WSN easily; resulting in overall device size shirking and hardware cost reduction. Although the DCO is suitable for biotelemetry applications, it still needs to further reduce power consumption, increase delay resolution, and extend frequency range.

In this paper, a high-resolution, wide-range and low-power clock generator is proposed for biotelemetry applications. The proposed DCO employs a cascade-stage structure to achieve high resolution and low power at the same time. In addition, the proposed DCO architecture not only can be implemented by all-digital CMOS design manner for cost and power reduction, but also can be described by hardware description language (HDL) and implemented with standard cells, making it easily portable to different processes and very suitable for biomedical chip applications and system integration.

2. Proposed Design

Figure 3 illustrates the architecture of the proposed DCO which consists of a coarse-tuning stage (CTS), 1st and 2nd fine-tuning stage (FTSs). To preserve the control code resolution and operation range, the proposed DCO employs a cascading structure to maintain control code resolution and extend operation range easily. The coarse-tuning stage and fine-tuning stages can extend operation range and improve the delay resolution, respectively. Because the requested lowest output frequency in the system is 10MHz, the conventional delay line structure is not suitable for this application. Thus, the proposed DCO employs a Schmitt-trigger-based delay cell (STDC) to generate a low-frequency clock with a low hardware cost in CTS[3]. Because the resolution of the CTS is not sufficient for typical DCO applications, two FTSs are added to further improve overall delay resolution of DCO.

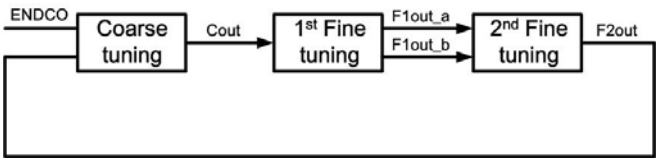


Figure 3. Block diagram of the proposed DCO.

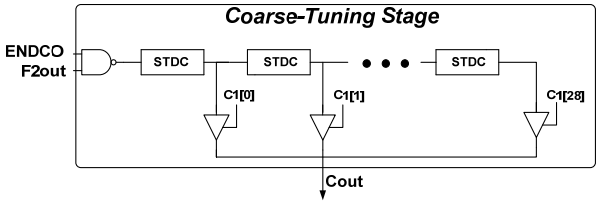


Figure 4. Circuit diagram of the proposed CTS.

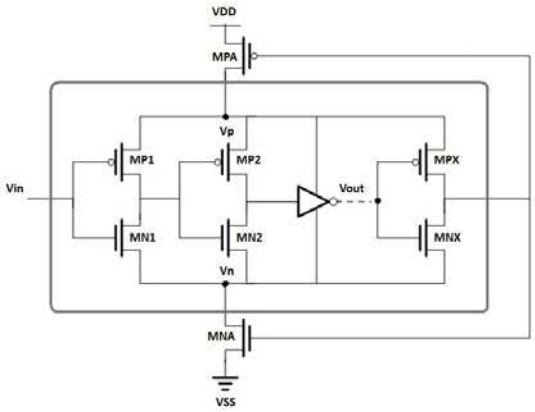


Figure 5. Circuit diagram of the proposed STDC.

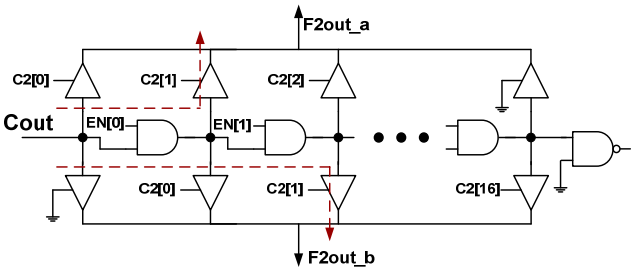


Figure 6. Circuit diagram of the proposed 1st FTS.

Figure 4 shows the circuit of the coarse-tuning stages. There are 29 different delay paths in the CTS and only one path is selected by the path selector tri-state buffers controlled by coarse delay control code (C1[28:0]).

The circuit diagram of the proposed STDC is shown in Figure 5. The Boolean function of STDC is the same as that of a normal inverter, except the hysteresis property induced by a Schmitt trigger [3]. Because the STDC can provide larger delay as compared with the conventional delay cell, it can replace numbers of delay cell leading to reduce power consumption and chip area.

The proposed 1st FTS is designed based on delay-path selection structure and the segmental delay line [9], as shown in Figure 6. According to the 1st FTS control signals (C2[16:0), the 1st FTS generates two output signals F1out_a and F1out_b for 2nd FTS. The 1st FTS control signals are the one-shot code, thus only one pair output signals will be generatd. The delay difference between these two output signals us one AND gate delay. For example in Figure 6, if C2[1] is high level, the propagation delay from Cout to F1out_a is one AND gate delay, and from Cout to F1out_b is two AND gate delay. In addition, this structure can disable not-working delay cells when the enable signals EN[16:0] are equal to low level. Moreover, in order to balance the delay step of 1st FTS, it has to add one dummy AND gate in the end of the delay chain.

The design challenge of the fine-tuning stage is how to improve delay resolution while keeping delay monotonic characteristic. The delay interpolator structure uses two driving groups that are controlled by two complementary codes to perform a delay interpolation [10]. The 2nd FTS is composed of interpolator structure to improve delay

resolution as shown in Figure 7. According to the 2nd FTS control signals (C3[16:0)], the 2nd FTS can generate the delay step with 1/16 of 1st FTS. As a result, the overall delay resolution can be further improved while keeping delay monotonic characteristic.

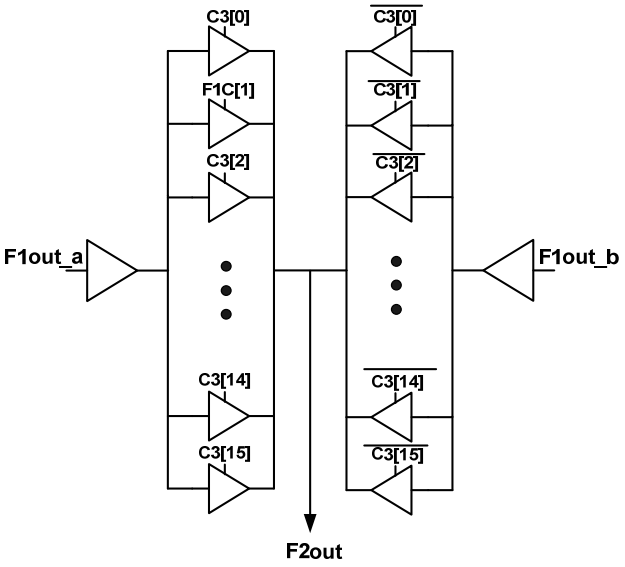


Figure 7. Circuit diagram of the proposed 2nd FTS.

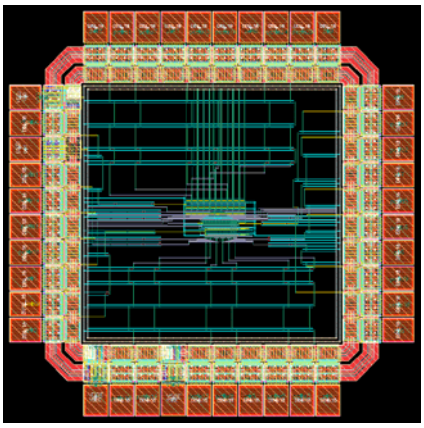


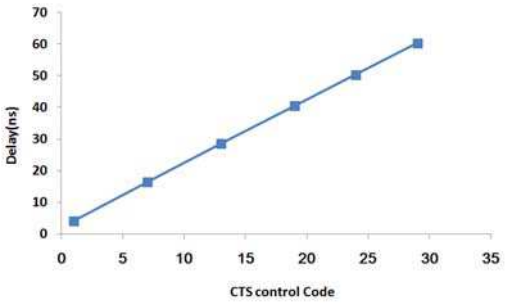
Figure 8. Test chip layout

3. Simulation Results

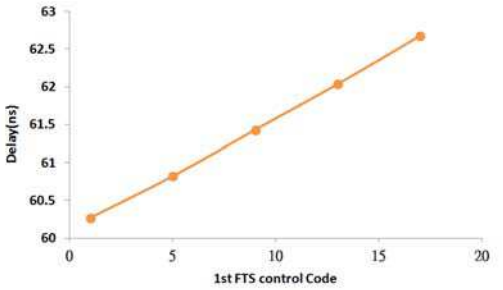
The proposed DCO is designed and implemented by 0.18μm 1P6M CMOS standard cell library and cell-based design flow. The layout of DCO test chip is shown in Figure 8. The post-layout HSPICE simulation results of controllable delay range and the finest delay step of different tuning stages are shown in Table 1. Because the finest step of 2nd fine-tuning stage determines the DCO resolution, the proposed DCO can achieve high resolution with 10.5ps. It should be noted that the controllable delay range of each stage is larger than the finest delay step of the previous stage. As a result, the cascading DCO structure does not have any dead zone larger than the LSB resolution of DCO.

Table 1 Simulation results of step/range of tuning ranges

	CTS	1st FTS	2nd FTS
Step(ps)	2004.6	150.5	10.5
Range(ps)	56130.1	2407.9	168.5



(a)



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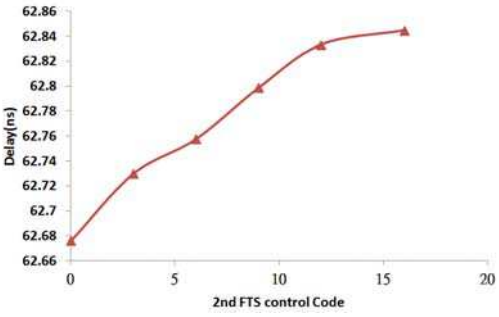

(c)

Figure 9. Simulation results of (a) CTS, (b) 1st FTS, and (c) 2nd FTS.

Table 2 Performance Summary

Performance Indices	Proposed DCO
Process	0.18μm CMOS
Operation (MHz)	7.9 ~ 120.8
LSB Resolution (ps)	10.54
Power Consumption (mW)	0.054@7.9MHz 1.435@121MHz
Portability	Yes

Figure 9(a), (b), and (c) shows CTS, 1st FTS and 1st FTS code-to-delay simulation results, respectively. The power consumption, frequency range and delay resolution of proposed DCO is 54 μW @ 7.9 MHz, 7.9~120.8 MHz and 10.5ps. The performance summary of the proposed DCO is shown in Table2.

4. Conclusions

In this paper, we have proposed a high-resolution and wide-range, and low-power DCO with cell-based design for biotelemetry applications. The proposed DCO employs a cascade-stage structure including, CTS, and FTS to achieve high timing resolution and wide frequency range at the same time. Besides, based on the STDC, the proposed clock generator can generate low frequency clock signal with low power consumption and low circuit complexity as compared with conventional approaches. Moreover, because the proposed DCO has a good portability as a soft intellectual property (IP), it can reduce both design time and complexity. As a result, it is very suitable for System-on-Chip (SoC) applications as well as system-level integration.

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