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A Wide Frequency PLL-less Clock Generator with Fast Intermittent Operation for Low-Power Wearable Medical Applications

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***Abstract*—A Wide Frequency PLL-less Clock Generator with Fast Intermittent Operation is presented in this paper to replace both the external frequency reference and PLL combination used in current wearable medical devices. The system uses one loop to stabilize the amplitude and the other to stabilize the slope of a saw-tooth signal to generate stable frequency over a wide range. Measurement results from a chip fabricated in 180nm CMOS process gives a linear frequency range of 0.1MHz-10MHz and 7us settling time without using a PLL. The total power consumption is 360uW that includes output buffers and external current sources with ±0.84% variation in frequency from 0-70 degrees. Using the proposed system as a clock generator for microcontrollers used in current wearable medical devices, would result in a one or more order of magnitude reduction in power consumption.**

I. Introduction

The cost of medical care is increasing rapidly due to many factors like long life expectancy and aging population around the world. One of the solutions for providing better medical services at reduced cost is through the use of wearable medical devices as shown in Fig.1. These devices will remotely monitor various vital signs and provide feedback to the physician in real time without the need for the patient to be in the hospital. Since these devices are attached with the patient all the time, power consumption should be minimized to minimize size, weight and battery maintenance. Current microcontrollers used in medical devices use dynamic voltage and frequency scaling (DVFS) for power consumption reduction [1] [2]. The frequency is swept from few hundred KHz to 8 or 16MHz, depending on the supply. Consequently, clock frequency is increased if the person is in critical condition for intensive monitoring and decreased otherwise to prolong battery life. Such microcontrollers use a combination of a crystal or an on-chip reference generator with a PLL to generate clock frequencies over a wide range. However, the long startup time and high power consumption for such a combination will make it difficult to realize many applications especially those requiring high intermittent rate. In this work, a stabilized on-chip reference oscillator that can be linearly programmed over a wide frequency range with fast settling time is proposed. The proposed system does not require a PLL in the microcontroller to generate a wide frequency range thus it greatly saves power consumption.

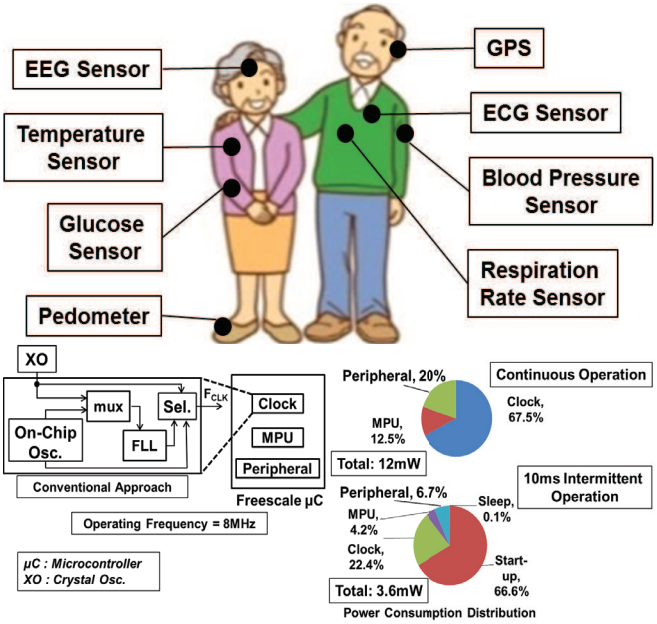

Fig. 1: Various applications of wearable medical devices and power consumption breakdown for microcontrollers used in them

II. Wide Range Frequency Generation for Sensor Nodes

The microcontroller used in wearable devices operates most of the time especially for applications requiring high intermittent rate. The bottom of Fig.1 shows the power consumption distribution of a low power microcontroller. It shows that significant amount of the power is consumed in clock generation and clock startup during continuous and intermittent operation, respectively. Therefore, to reduce such power consumption, on-chip reference oscillators are used instead of crystals due to their low power consumption and fast startup time. However, most of the previously reported on-chip reference oscillators were designed to generate a single frequency. They use an

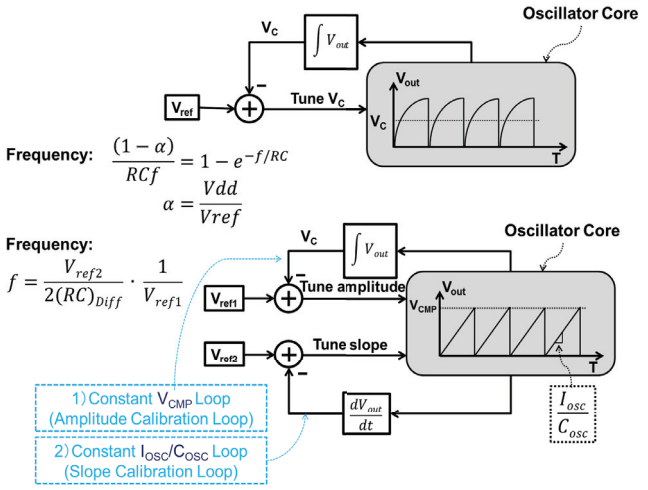

Fig. 2: The conventional and the proposed system concept diagram showing the non-linear change in frequency for the conventional and the liner change in the proposed system

RC relaxation oscillator core with feedback to stabilize the frequency [3] [4]. The feedback adjusts the comparator threshold to compensate PVT variations as shown in the top of Fig.2. Varying the frequency for such topology is difficult since the frequency varies non-linearly with change in the reference or RC constant as shown in the equation in the top of Fig.2. Therefore, most work adopting such architecture is tailored for a single frequency output and needs a PLL. The work in [5] [6] allow for frequency variation however only discrete frequency steps are obtained and a PLL is included on chip in [5]. They also require long calibration and consume considerable power and area [7].

III. Wide Frequency Range Dual-Loop On-Chip Oscillator

A. Concept

The proposed system uses a relaxation oscillator core that generates a saw-tooth signal with dual feedback loops to stabilize the frequency. The frequency of the core alone is ideally determined by the current source and capacitor Cosc . However, temperature and voltage variations introduce variation in the comparator delay and in the current source that is charging Cosc and thus affects the frequency. To stabilize the frequency against temperature and voltage variations, two feedback loops are used. One loop stabilizes the amplitude of the saw-tooth while the other stabilizes its slope. The combination of both loops stabilizes the frequency as shown in the equation at the bottom of Fig.2. The equation does not depend on the comparator delay or the value of the current that is charging Cosc. It only depends on Vref1, Vref2 and the RC constant of the differentiator circuit. Consequently, temperature and supply variations effects are minimized. Also, the amplitude can be maximized for good SNR while the slope can be varied to change the output frequency over a wide range. Moreover, from the bottom frequency equation in Fig.2,

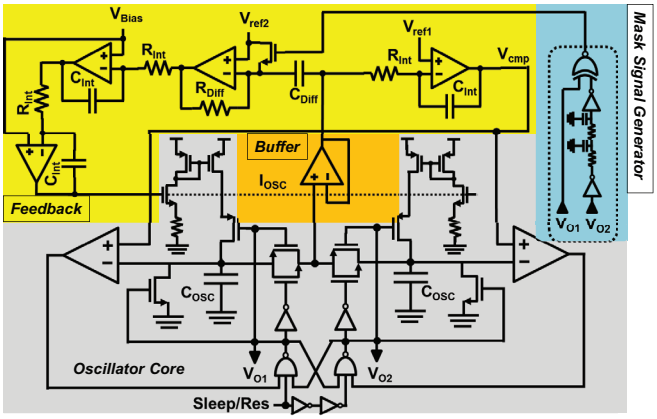

Fig. 3: Detailed schematic of the proposed system showing various major blocks in different colors

it can be seen that the frequency changes linearly with the slope reference voltage making it suitable for replacing both the reference frequency and the PLL combination in many systems.

B. Circuit Implementation

A detailed schematic of the proposed system is given in Fig.3. The core oscillator circuit consists of an SR latch along with two comparators, current sources, Cosc capacitors and switches as shown in the greyed area. A buffer is used to isolate the feedback circuit from the core oscillator circuit as shown in the orange area. Two feedback loops are used to stabilize both the slope and amplitude of the saw-tooth wave signal are shown in the yellow area in Fig.3. The slope calibration loop is made much faster than the amplitude calibration loop to avoid instability issues. The amplitude stabilization feedback uses an integrator to control the threshold of the comparator thus maintaining the amplitude. The slope calibration part differentiates the signal to extract the slope information (defined as IOSC/COSC) and integrates the error signal which controls the current charging the capacitor thus maintaining a constant slope. The discontinuity in the slope that appears every period causes the differentiator circuit to produce an undesired pulse at the beginning of each period which affects the accuracy of the system. To reduce this effect, a new differentiator circuit is proposed in which a masking signal is used to pre-charge the differentiator capacitor to Vref2 at the beginning of each period. The masking signal is generated from the core oscillator using the circuit shown in the blue area in Fig.3. It takes the two differential outputs, delay one of them and perform an XOR on the result to generate the masking signal. This minimizes the undesired pulse and improves the accuracy of the system.

IV. Measurment Results

The system is fabricated in 180nm CMOS process occupying an area of 0.038mm2 as shown in Fig.8. It is measured with a 2V power supply and has a power consumption of

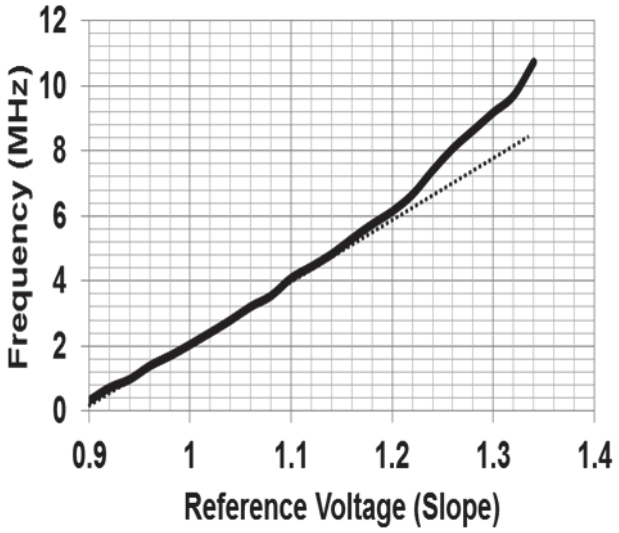

Fig. 4: Measurements showing output frequency vs reference voltage

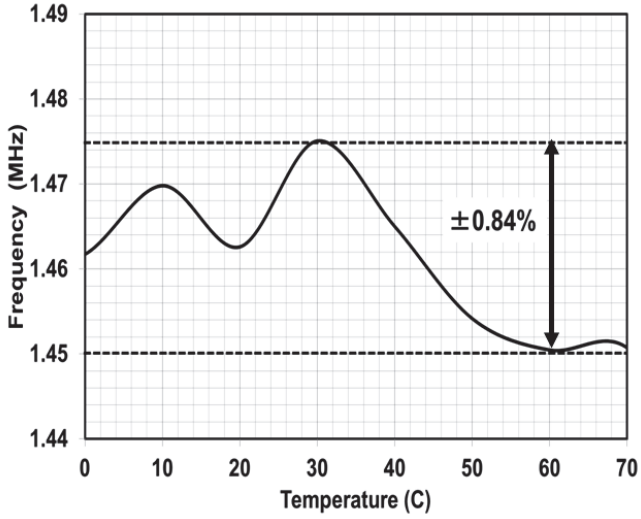

Fig. 6: Measurements showing that the variation of frequency with temperature

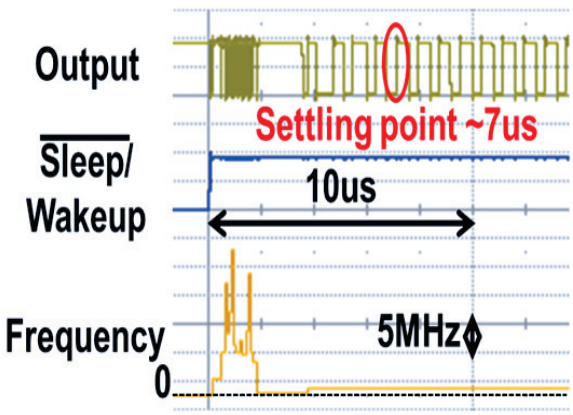

Fig. 5: Measurements showing settling time from the moment the system is started

	This Work	[5]*	[6]	[3]	[4]	[7]
Process [nm]	180	180	250	180	130	65
Supply [V]	2	3.3/1.8	2.5	1.8	1.5	1.2
Oscillator Topology	Relaxation	Relaxation	LC	Relaxation	Relaxation	Relaxation
Frequecy [MHz]	0.1 - 10	2-40	0.5-480	14	3.2	12.6
Frequecy Sythesis	Yes (continous)	Yes (40Hz Step)	No (Divider only)	No	No	No
Power Consumption [uW]	360	2900	49500	43	38.4	98.4
Settling Time [us]	7	3300000	100000 initial calibration	10	N/A	N/A
Variation with Temp (C) %	±0.84 (0 - 70)	±0.0085 (0 - 70)	±0.006 (0 - 70)	±0.75 (-40 - 125)	±0.25 (20 - 60)	±0.82 (0 - 80)
Variation with VDD %	±1.5 (1.94-2.06V)	±0.003** (3.63-2.97V)	±0.001** (3.63-2.97V)	±0.16 (1.7-1.9V)	±0.4 (1.4-1.6V)	±0.07 (1.1-1.5V)
Area [mm^2]	0.038	1.04	2.25	0.04	0.073	0.01

*PLL is included on chip ** LDO is present

Fig. 7: Performance comparison of this work to latest publications

380uW including output buffers and external current sources. Most of the core power is consumed by the OpAmps in the feedback circuits and therefore there is negligible change of power consumption with frequency. Fig.4 shows the change of frequency with the slope reference voltage (Vref2). As predicted by the equation in Fig.2, the frequency changes linearly with the change in the slope reference voltage from 0.1MHz to 10MHz. Above 6MHz, gain-bandwidth limitation of the isolation buffer introduces some nonlinearity in the tuning which can be fixed by an improved buffer topology. Fig.5 shows that it takes the oscillator about 7us to reach a stable operation from the moment the wakeup signal becomes high making the system suitable for high intermittent rate applications. Fig.6 shows the stability of the system with temperature variations where the system achieves 0.84% variation in frequency from 0-70 degrees. The proposed system also achieves 1.5% variation in frequency with change in supply voltage from 1.94-2.06V (76% improvement in comparison to the oscillator with no feedback). Performance comparison to state of the art work is given in the table in Fig.7. The table shows that the proposed system has about 10 times lower power consumption than [5] and 100 times lower than [6] with a similar tuning range. Other work would require frequency extension circuits to generate a variable frequency which would increase power consumption. Moreover, fast start up time allows long sleeping interval in intermittent operation for further power consumption reduction.

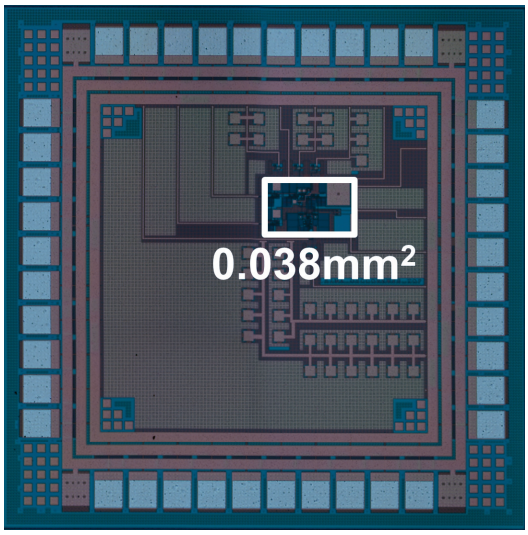

Fig. 8: Chip photograph of the proposed system

V. Conclusion

Wearable medical devices are spreading rapidly due to population aging in order to reduce medical costs. These devices are mostlyl battery-powered thus power consumption should be minimized. Most of the power in these devices is consumed by RF transmission and microcontroller. The power consumption of RF transmission can be reduced through long intermittent operation. However, the microcontroller work most of the time to monitor vital signs and therefore long intermittent operation is not feasable. Therefore, this paper proposes a stable on-chip CMOS oscillator for crystalless wearable medical applications. The system can be tuned linearly from 0.1 to 10 MHz making it suitable for replacing both the external crystal oscillator and the PLL in generating a stable clock signal for the microcontroller. Moreover, dynamic frequency scaling can be easily implemented to adjust the responce of the system on demand due to the fast settling time of 7us.Therefore, low power in combination with fast startup for intermittent operation makes the proposed work capable of one or more order of magnitude reduction in the power consumption for wearable devices if it is to be used for clock generation in microcontrollers (e.g., the one in Fig.1).

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