A Novel Neural Network Ternary Arithmetic Logic Unit

Ali Haidar[†], M. Jad Hamdan[†], M. Backer Rashid[†], Hassan Hamieh[†], Ahmad Issa[†], Abdallah Kassem[††]
† Department of Computer Engineering and Informatics, Beirut Arab University
† P.O. Box: 11-5020, Beirut, Lebanon
†† Department of Electrical and Computer Engineering, Notre Dame University, Zouk, Lebanon
† ari@bau.edu.lb, jadhamdan@gmail.com, backer.rashid@gmail.com, eng.hasanhamieh@gmail.com,
eng.ahmadissa@gmail.com, †† akassem@ndu.edu.lb

Abstract: in this paper we introduce a new set of ternary neural networks to realize a novel Ternary Arithmetic Logic Unit (TALU). All the neurons take advantage of the Logic Oriented neural network mathematical tools and parallelism concepts allowing fast and simple systematic analysis. The simulation results, done using MATLAB Simulink, demonstrate the feasibility, functionality and the correctness of the neural networks designed.

1. Introduction

Artificial neural networks are receiving widespread attentions as potential new architectures for computing systems. Many models have been reported concerning neural networks. However, the research on neural network model has focused mainly on theoretical studies and computer simulations. Several groups have initiated experiments with VLSI implementations and demonstrated a few functional circuits.

Artificial neural networks contain highly interconnected processing elements called neurons. The proposed neural network is a multiple-valued logic (MVL) neural network, and is called Logic Oriented (LOGO) Neural Network. The MVL is expected to be the technology of the future [1-6]. The neural networks proposed are composed of a large number of highly interconnected processing elements (neurons) each having n-inputs. The links' weights and thresholds are two types: Real number weights and variable weights (dynamic weights); such weights facilitate network optimization and hardware implementation. The neural networks designed have been simulated using MATLAB Simulink. The simulation results demonstrated the feasibility, functionality, and the correctness.

2. Ternary model neuron and its firing rule

Figure 1 shows the neuron model for the proposed artificial neural networks. The weighted inputs to a neuron are accumulated and then passed to an activation function (Figure 2) which determines the neuron response.

In this paper, a new activation function for multiple-valued logic (MVL), specifically for ternary system is introduced. It is called the Ternary Activation Function (TAF), and defined as follow:

$$f(Z)=\begin{cases}0 & if \quad Z<0\\ 1 & if \quad 0\le Z<2\\ 2 & if \quad Z\ge 2\end{cases}$$

Where, $f(Z)$: Output of the processing element,
$Z = \sum x_i\, w_i + \theta$,
x_i: input signals,
θ: threshold,
w_i: coefficient weights,
$i = 1, 2, \ldots\ldots, n$

3. Neural Network of Ternary Arithmetic Logic Unit

The Ternary ALU is a breakthrough not only because we can control more functions in the same number of control lines, but it can perform faster than a binary ALU and it can be the first stone in the switching from binary to MVL [2, 6], ternary systems in this paper. The proposed block diagram is a 1-trit TALU that includes many arithmetic and logic functions as given in Figure 3. The TALU functions are listed in Table 1, where the Table 2 represents the truth table for all proposed ternary functions. The TALU performs an operation, and the result of this operation should be transferred to a destination ternary register. The transfer operation from the input, through the TALU, and into the output is performed correctly as illustrated in the simulation of Figure 5.

The TALU's architecture of Figure 3 shows one stage of the logic circuit. It consists of nine ternary arithmetic and logic functions and a 9-to-1 multiplexer. The neural networks of these ternary functions and the multiplexer have been designed as illustrated in Figure 4. The output of these ternary functions are applied to the input of the multiplexer with two selection variables (control lines) S_0 and S_1. Table 1 lists the arithmetic and logic operations obtained for each combination of the selection variables.

The neural networks of all the ternary functions and the multiplexer of Figure 4 constitute the neural network of the TALU. The complete neural network of the TALU has been simulated using MATLAB Simulink, where the simulation results of Figure 5 demonstrated the feasibility, functionality, and the correctness. Note that, we are still working to improve the simulation from the view point of delay and to remove the glitches.

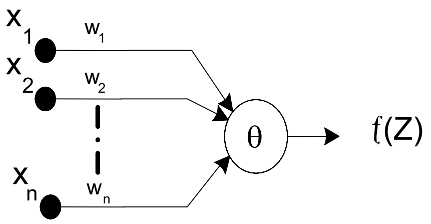


Figure 1: Processing element.

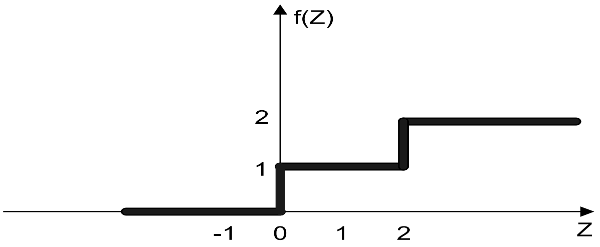


Figure 2: Ternary Activation Function.

Table 1: TALU functions, and function Table

Name	Main effect	Number of inputs	Used Weights		notes	Control Signals	
			Real numbers	Dynamic		S_0	S_1
Add	Addition	2 inputs	√		Newly proposed	0	0
Multiply	Multiplication	2 inputs	√	√	Newly proposed	0	1
Magnitude	Magnitude	2 inputs	√		Newly proposed	0	2
Min	Minimum	2 inputs	√	√	Newly proposed	1	0
Max	Maximum	2 inputs	√			1	1
Ex- Max	Exclusive-Maximum	2 inputs	√		Newly proposed	1	2
Rotate-up	Rotate-up	1 input	√		Newly proposed	2	0
Rotate-down	Rotate-down	1 input	√		Newly proposed	2	1
Invert	Complement	1 input	√			2	2

Table 2: The truth table of the TALU functions.

A	B	Add	Multiply	Magnitude	Min	Max	Ex-Max	Rotate Up (A)	Rotate Down (A)	Invert (A)
0	0	0	0	1	0	0	0	1	2	2
0	1	1	0	2	0	1	1			
0	2	2	0	2	0	2	2			
1	0	1	0	0	0	1	1	2	0	1
1	1	2	1	1	1	1	0			
1	2	0	2	2	1	2	2			
2	0	2	0	0	0	2	2	0	1	0
2	1	0	2	0	1	2	2			
2	2	1	1	1	2	2	0			

Figure 3: Block Diagram of the proposed TALU.

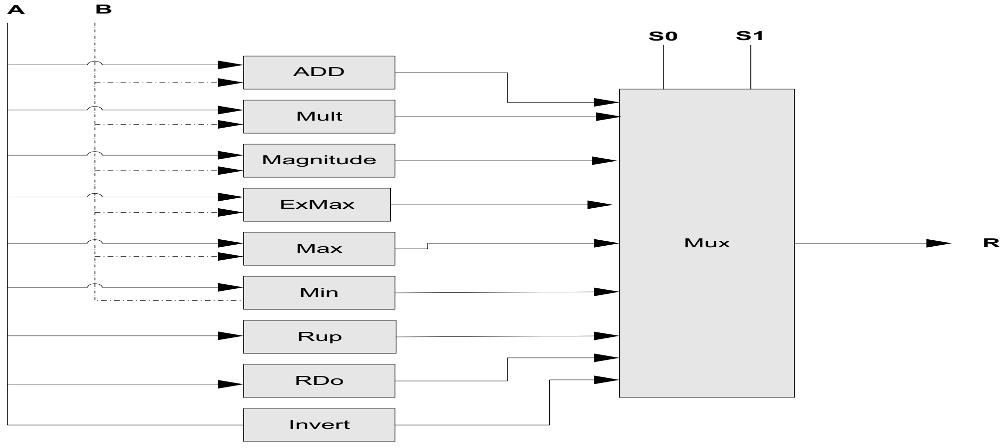
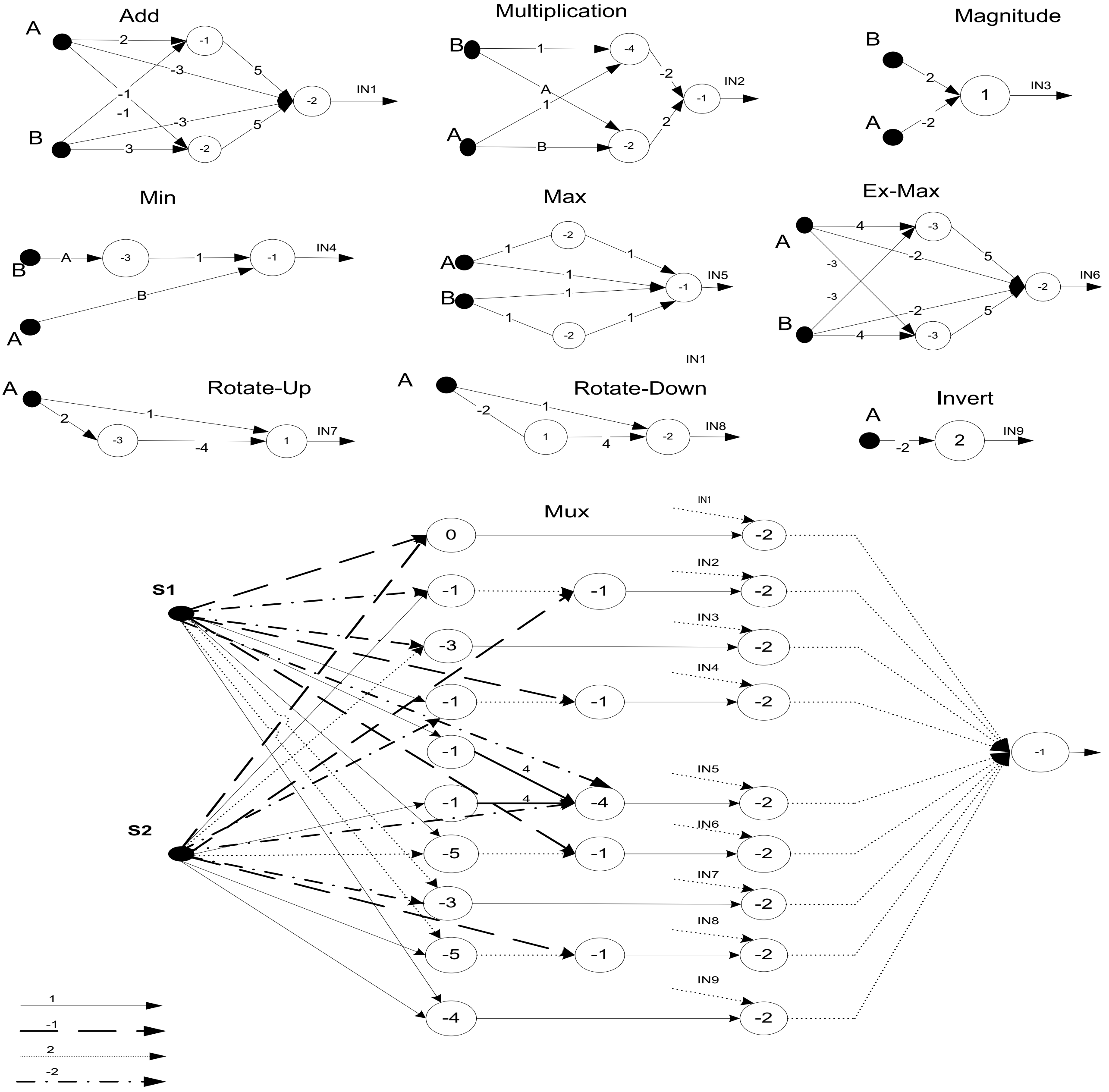


Figure 4: Neural networks of the TALU ternary



4. Comparison between the TALU and a binary ALU

TALU can control more gates with the same number of control lines that a binary ALU has; due to the implementation of the 3-Valued Logic in it.

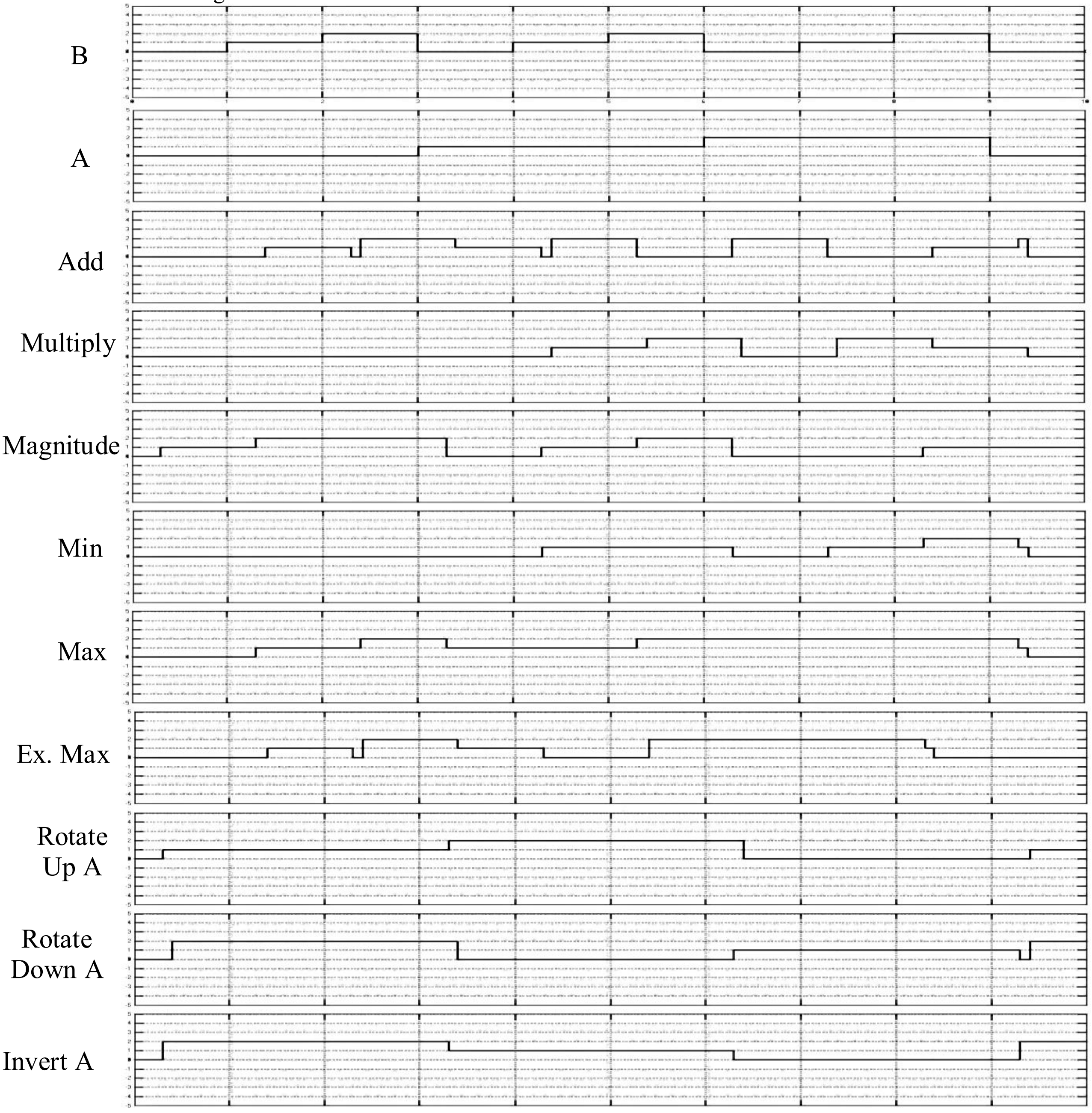
TALU, because of the previously mentioned point it would cause less power consumption when it will be implemented in hardware.

TALU operates faster than a binary ALU because the clock cycle has three states while one clock cycle in a binary ALU has only two states, so tuning a ternary clock to have the same frequency of a binary clock will definitely produce faster systems because instead of covering 2 states in a cycle, it covers 3 states.

5. Conclusion

We conclude that the TALU implemented using the uprising electronics architecture of the Artificial Neural Networks will be a more efficient and faster ALU. Furthermore, we'll have much more functions with less number of control signals, thus less wiring. This will lead to less power consumption. When embedding the TALU in a complete ternary microprocessor we'll have a breakthrough in the computing hardware field.

Figure 5: MATLAB Simulink simulation results of the Neural Network of the TALU.



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