A Nanopower Full CMOS Sub-Bandgap Voltage Reference

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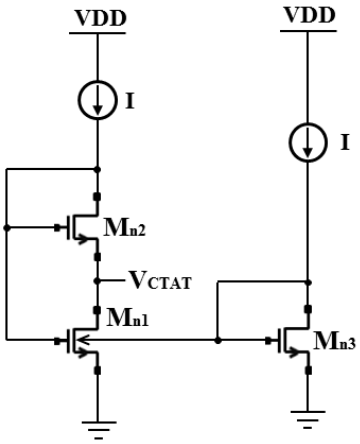
Abstract: This paper describes a sub-1V nanopower full CMOS bandgap reference (BGR) operated in subthreshold region. Complimentary to absolute temperature (CTAT) voltage generator was realized by using two n-MOSFET pair with body bias circuit to make a sufficient amount of CTAT voltage. Proportional to absolute temperature (PTAT) voltage was generated from differential amplifier by using different aspect ratio of input MOSFET pair. The circuits are implemented in 0.18um CMOS process. The simulation results show that the proposed sub-BGR generates a reference output voltage of 358mV, obtaining temperature coefficient of 32 ppm/C in -40°C to 120°C of temperature range. The circuits consume 43nW at 1V supply and operation range is 0.65 to 1.8V.

Keywords-- **Bandgap voltage reference, BGR, subthreshold, reference circuit, nanowatt**

1. Introduction

As the development of Internet of Things (Iot) and wireless systems, the need for designing low voltage and low power bandgap voltage reference grows fast. As this trend, several bandgap reference (BGR) circuits have been released. The resistor-less voltage reference that operates in nano-watt power consumption with one bipolar transistor has been reported [1]. However, the bipolar transistor occupies larger area than MOSFET and needs an additional mask layer. A sub-1V full CMOS voltage reference circuit that is based on gate-source voltage of MOSFET to generate complementary to absolute temperature (CTAT) voltage is published [2]. However, the reference voltage changes significantly with process variations. Another BGR [3] uses body bias technique to reduce process variation and the proportional to absolute temperature (PTAT) voltage (ΔVgs) is generated by n-MOSFET pair with different oxide thickness. However, the circuit is very restrictive to apply on systems due to very low output reference voltage and also it needs a current trimming for further reducing the voltage change due to process variations. In this paper, to solve above problems, we present a new sub-1V full CMOS bandgap voltage reference which consumes few tens of nano-watt with very small variations among the significant variations of temperature, supply voltage and process.

This paper organized by follows: Section II presents the operational principle of CTAT voltage generator and PTAT voltage generator. Proposed sub-BGR circuits are described in section III. Section IV shows the simulation results of proposed BGR. Conclusions are given at section V.



Mn1, Mn2, Mn3 : Sub threshold
Mn1, Mn3 : High Vth (High voltage MOSFET)
Mn2 : Low Vth (Low voltage MOSFET)
Fig. 1. Proposed CTAT voltage generator

2. Operation Principles

2. 1 CTAT voltage generator

In conventional BGR circuits, CTAT voltage is created by the base-emitter voltages (VBE) of bipolar junction transistors or the threshold voltages (Vth) of MOS transistors. However, VBE and Vth are variable parameters following process variations. Particularly, Vth largely changes depending on process variations. As the result, the variation of CTAT voltage will affect output reference voltage. In recent reported sub-BGR circuits [2] [6], the architecture as shown in Fig. 1 is usually adopted for generating a process invariant PTAT voltage. However, we modified the architecture to have CTAT behavior to apply to our overall circuit design as will be shown later. However, process variations partially remain in the circuit [7] since the threshold voltage of Mn1 (HVTMOS) and Mn2 (LVTMOS) change differently by process variations as will be shown later. Therefore, we adopted body bias circuit to reduce process variations caused by ΔVth between Mn1 and Mn2. Fig. 1 shows proposed architecture of CTAT voltage generator. Mn1 is a high voltage MOS transistor and Mn2 is a low voltage MOS transistor. The calculation of VCTAT is shown below.
The subthreshold current for a drain-source voltage of MOSFET can be expressed as

$$I_{ds} = \mu C_{ox}(\eta-1)V_T^2\left(\frac{W}{L}\right)\exp\left(\frac{V_{gs}-V_{th}}{\eta V_{th}}\right)\left[1-\exp\left(-\frac{V_{ds}}{V_T}\right)\right] \quad (1)$$

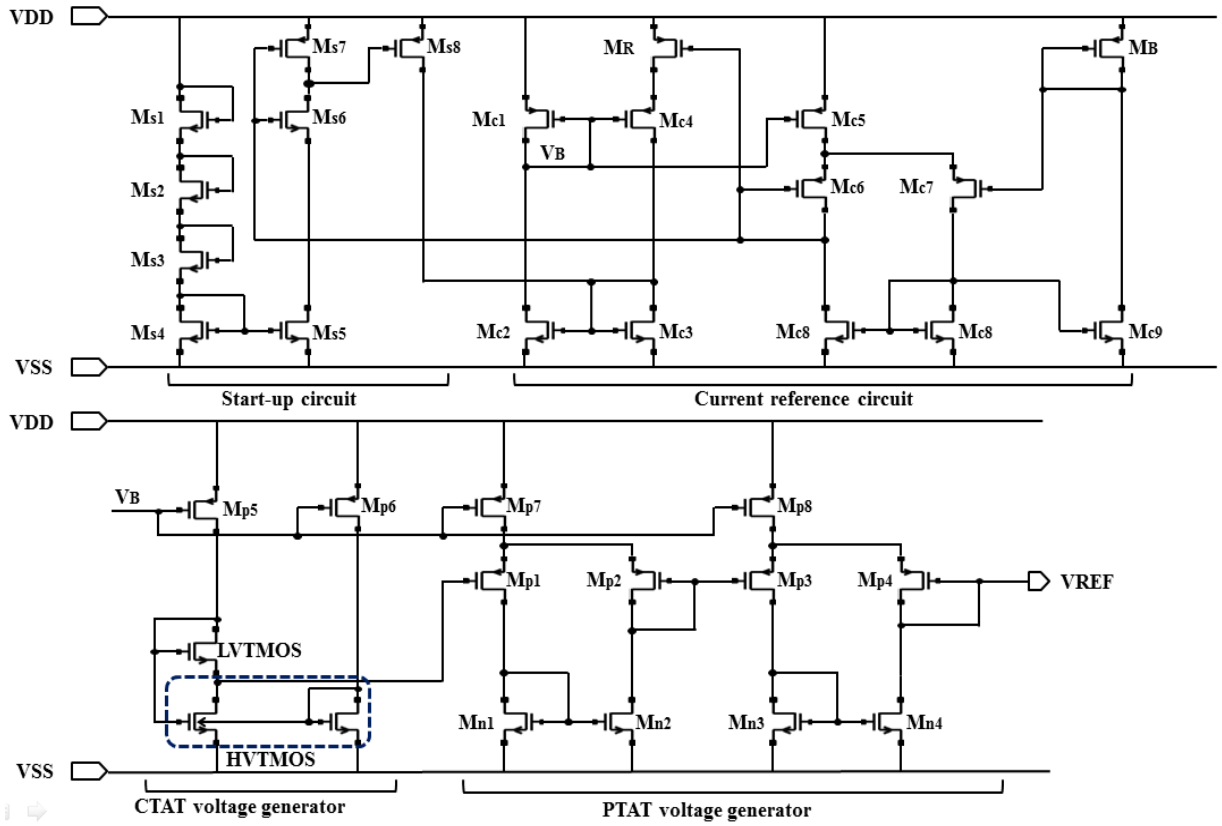


Fig. 2. Schematic of proposed sub-BGR

Where μ, C_{ox}, η, V_T, W/L, V_{gs} and V_{th} represent carrier mobility, gate-oxide capacitance, subthreshold slope factor, thermal voltage, aspect ratio, gate-source voltage and threshold voltage respectively. When $V_{ds} >> V_T$, Eq. (1) can be deduced as

$$V_{gs} = V_{th} + \eta V_T \ln\left(\frac{I_{ds}}{\mu C_{ox}(\eta-1)V_T^2\left(\frac{W}{L}\right)}\right) \quad (2)$$

Therefore, ΔV_{gs} between M_{n1} and M_{n2} can be calculated by

$$\Delta V_{gs} = V_{CTAT} = V_{gs,Mn1} - V_{gs,Mn2} = \left(V_{th,Mn1} - V_{th,Mn2}\right) + \eta V_T \ln\left(\frac{t_{ox,Mn2}\left(\frac{W}{L}\right)}{t_{ox,Mn1}\left(\frac{W}{L}\right)}\right) \quad (3)$$

Assuming the same size of both transistors and the difference of threshold voltage between the high voltage MOS transistor (M_{n1}) and the low voltage MOS transistor (M_{n2}), and since the voltage of second term is much smaller than the voltage of first term, Eq. (3) can be reduced as

$$V_{CTAT} \approx \left(V_{th,Mn1} - V_{th,Mn2}\right) \quad (4)$$

Eq. (4) presents CTAT behavior since positive threshold voltage difference shows negative voltage coefficient. Furthermore, supposing the same ΔV_{th} between M_{n1} and M_{n2} for each process corner, the variation of V_{CTAT} can be reduced even in the process variations

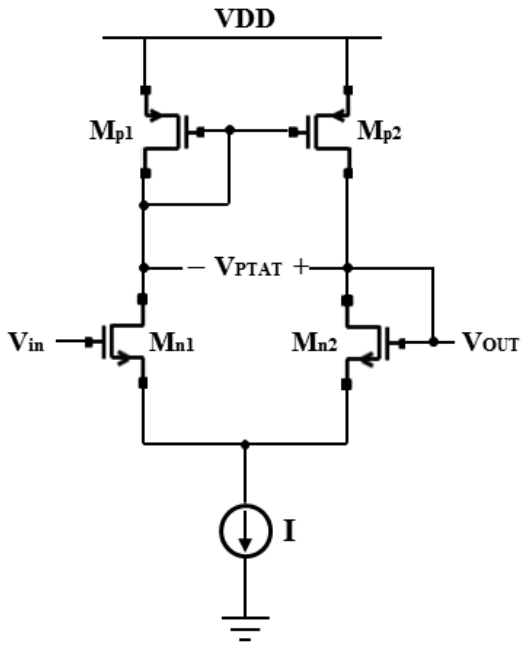


Fig. 3. PTAT voltage generator [5]

2. 2 PTAT voltage generator

Fig. 3 shows the PTAT voltage generator [5] which consists of a differential pair with a current mirror. The calculation of V_{PTAT} can be expressed as

$$V_{PTAT} = V_{in} - V_{out} = V_{gs,Mn1} - V_{gsMn2}$$

$$= V_{th,Mn1} - \eta V_T \ln\left(\frac{I_{ds,Mn1}}{I_0 K_{Mn1}}\right) - \left(V_{th,Mn2} + \eta V_T \ln\left(\frac{I_{ds,Mn2}}{I_0 K_{Mn2}}\right)\right) \quad (5)$$

Where I_0, and K represent $\mu C_{ox}(\eta-1)V_T^2$ and aspect ratio. Assuming the same V_{th} and the same current of differential input transistor pair, Eq. (5) can be simplified as

$$V_{PTAT} = \eta V_T \ln\left(\frac{K_{Mn1} K_{Mp1}}{K_{Mn2} K_{Mp2}}\right) \simeq \eta V_T \ln\left(\frac{K_{Mn1}}{K_{Mn2}}\right) \quad (6)$$

Therefore, PTAT voltage can be generated by setting $K_{Mn1}/K_{Mn2} > 1$.

3. Proposed BGR Circuits

Fig. 2 shows a schematic diagram of proposed sub-BGR. The current reference circuit [4] generates about 10 nA current and supplies it to the other parts of circuits. All MOSFETs are operated in subthreshold region except for MOS resistors (M_R, M_B) which are operated in the deep triode region. The currents flow through M_R and M_B are equal duo to the same aspect ratio. And the generated currents are robust to process variation because M_R and M_B are biased from the gate-source voltage of M_B and have the same threshold voltages. The CTAT voltage generator with body bias circuit to the body of Mn1 makes process invariant CTAT voltage. This CTAT voltage was connected to an input MOS transistor (V_{in}) of PTAT voltage generator. The two-stage PTAT voltage generator was designed to create the sufficient amount of PTAT voltage. Thus the temperature invariant output reference voltage can be generated.

4. Simulation Results

Simulations were performed with 0.18-um CMOS technology from a 1-V supply voltage. Fig. 4 and Fig. 5 show simulated CTAT voltage temperature behavior from the CTAT voltage generator according to the body bias circuit. The simulated values of ΔV_{CTAT} are 10mV and 5mV for each process corner respectively. The output reference voltage as a function of temperature is shown in Fig. 6. Simulation results show the small process variation of 5.4mV (1.508%) at each process corner. And 31ppm/°C, 41ppm/°C and 70ppm/°C on TT(typical-typical), SS(slow-slow) and FF(fast-fast) are resulted in the temperature range of -40°C to 120°C respectively. Fig. 7 shows the simulation results of proposed sub-BGR. The output reference voltage of 358mV is achieves in the supply voltage range from 0.65V to 1.6V. The simulated results of PSRR are 44dB at 100Hz for each process corner as shown in Fig. 8. To determine local mismatch effects, Monte Carlo simulation was performed as shown in Fig. 9 (σ/μ=1.54%). The power dissipation at 0.65V supply voltage was 23nW. Fig. 10 shows the layout result.

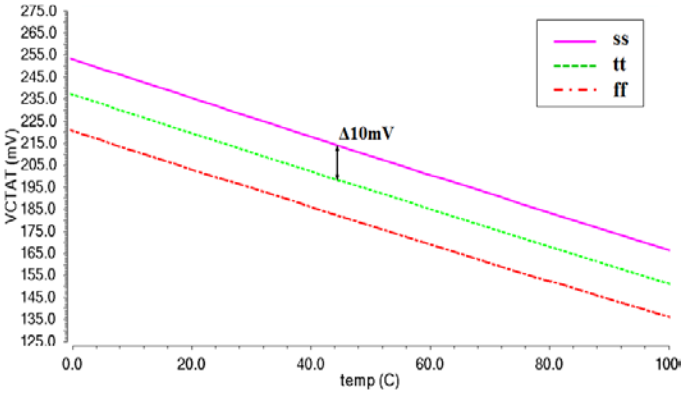


Fig. 4. CTAT voltage versus temperature w/o body bias

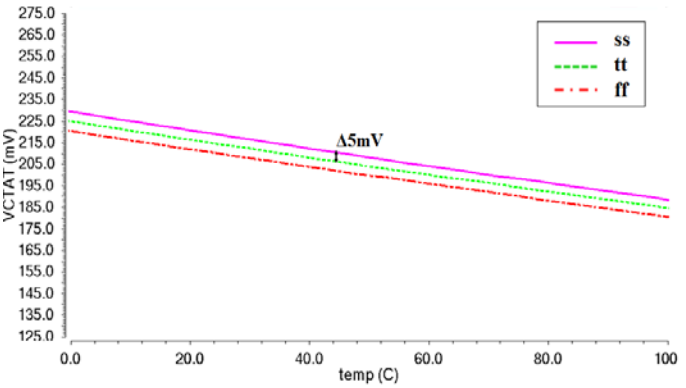


Fig. 5. CTAT voltage versus temperature w/ body bias

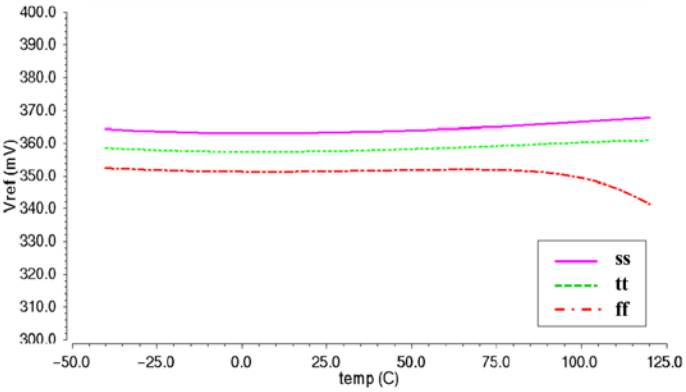


Fig. 6. Output reference voltage versus temperature

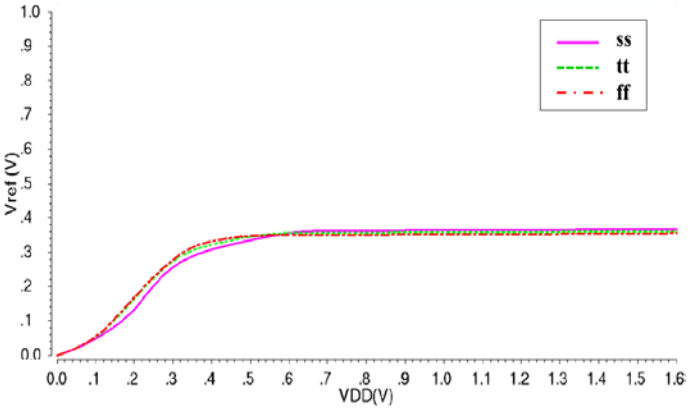


Fig. 7. Output reference voltage versus VDD

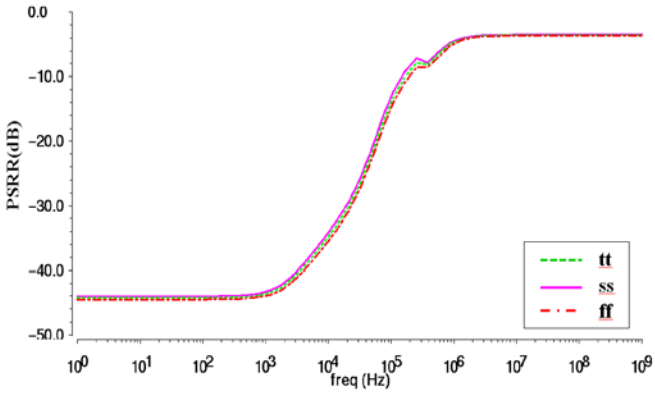


Fig. 8. Power supply rejection ratio

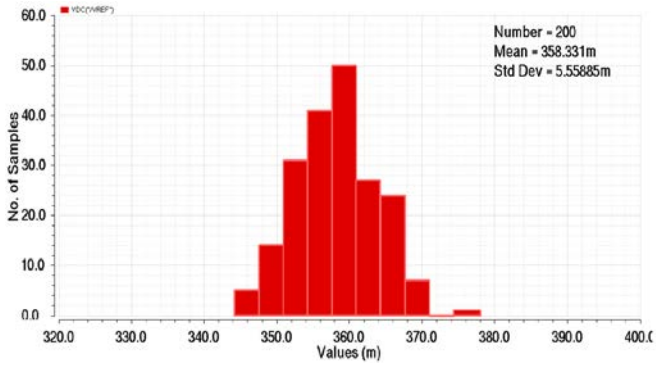


Fig. 9. Monte Carlo simulation for local mismatch

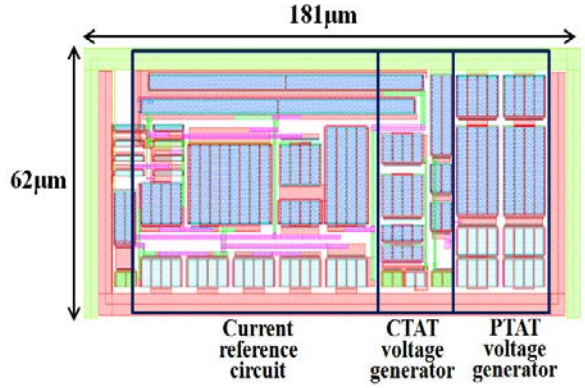


Fig. 10. Layout of proposed sub-BGR

5. Conclusion

Sub-1V BGR without BJTs and resisters is introduced. Two N-MOSFET pair with body bias circuit makes a sufficient amount of CTAT voltage. Differential amplifier configuration by determining different aspect ratio of input MOSFET pair generates PTAT voltage. And the circuits are robust from process variations by using the process invariant CTAT voltage. The simulation results demonstrated that the sub-BGR circuit could generate the output reference voltage of 358mV and the power dissipation at the room temperature was 23nW at 0.65-V supply voltage.

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