New Approach for Detection and Storage an ESD event by using ReRAM cell

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Abstract: This work proposes a new concept of a circuit that can detect an ESD (Electrostatic discharge) event and save the ESD level by using ReRAM cell. The circuit is configured such that an appropriate voltage level corresponding to the ESD level is applied to both ends of the ReRAM (Resistive random-access memory) cell in the circuit, when an ESD event occurs. Through this structure, the resistive state of the ReRAM cell is changed according to the voltage level. The ReRAM cell having a non-volatile characteristic can be maintained the resistance value changed in the ESD event regardless of the power state, and the ESD levels can be identified by the level of the resistance. Through the ReRAM modeling and the SPICE simulation, It is verified that the resistive state of ReRAM cell can be changed instantaneously under ESD event. Also, it is verified that the proposed circuit including ReRAM cell can detects and stores ESD events. Finally, by using the proposed circuit, a mothod of preventing the soft error caused by sytem level ESD in mobile device is introduced.

1. Introduction

Recently, IT trend is changing rapidly with the expansion of mobile applications such as an IOT (Internet of Things), a smart health-care and a mobile payment system. The combination of smart technology and mobile environments offers an undreamed convenience, but also has the risk of soft error due to a Set level ESD (Electrostatic Discharge) that occur during the basic operation such as charging the device, connecting with other devices, and carrying any where. The soft error refers to a temporary fault of the system as opposed to hard error, which means a permanent failure due to physical damage. In Figure 1, The type of failure that can occur in the various case of the ESD is shown, and It can be seen that the probability of a Soft failure in the Set level ESD is relatively higher than other cases.[1]

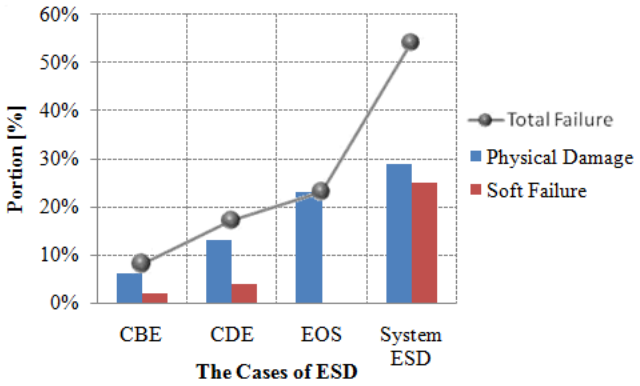


Figure 1. Type of failure in the various cases of ESD event: Charged Board Events (CBE), Cable Discharge Events (CDE), Electrical Over Stress (EOS), and System level ESD [1]

These soft errors cause the serious fault such as the malfunction of the system and the corruption of the stored data. In particular, because it can lead to a critical accident in systems that require high reliability, such as the medical, the financial, and the security field, the Technology for detecting these soft errors is absolutely necessary. The soft error in semiconductor devices are widely known to be occurred by the energy particles coming from outside such as an alpha particle, but the power fluctuation due to the external noise source such as Set level ESD is one of the causes. It has been reported that a soft error by the set level ESD can cause a malfunction in the mobile device. Also a circuit for detecting ESD event and protecting the malfunction has been proposed in [2]. But, because the circuit in order to store the detected ESD information operates only when power is applied, the device of the power-off state is not protected at an ESD risk.

A circuit that can protect the system from a soft error due to ESD without being affected by the power state is needed. This work proposes a circuit that detects the ESD event and can store the ESD information even in a power-off state using the ReRAM (Resistive random-access memory) cell to maintain stored data even when the power is disconnected.

ReRAM is the one of a promising technology for the next generation non-volatile memory due to low power consumption, high-speed operation, ease of fabrication, and high-density integration. ReRAM has a characteristic that is converted from a high resistive state (HRS) to a low resistive state (LRS) or vice versa by voltage applying across cell. [3] These characteristics of the ReRAM which changes the resistance depending on the applied voltage and maintains the changed value in power off state can be used as not only the storage features of the memory itself but also the special circuit that can store a voltage change occurred in the ESD event.

In this work, the circuit that can detect an ESD event and store the level of the ESD regardless of the presence or absence of power is proposed in the following sequence. First, through the modeling of TLP (Transmission Line Pulse) tester, the SPICE simulation method to represent the fluctuation of the power line due to ESD pulse is proposed. This is to faithfully reproduce the soft error due to the Set level ESD. And, the modeling result of ReRAM is introduced. Second, the circuit implementation for the detection and storage of ESD and the verification result is introduced. Finally, the consideration to use the information stored in the ReRAM is introduced and the conclusion of this work is summarized.

2. Circuit Implementation and Verification

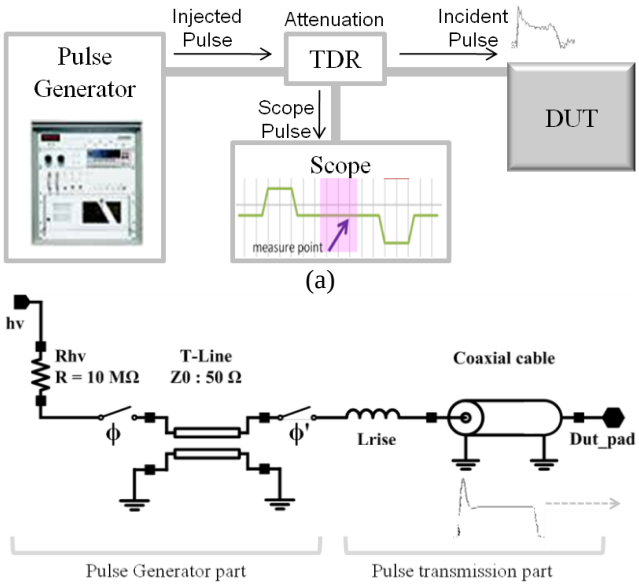


Figure 2. (a) The diagram of TLP Tester for ESD test, and (b) the schematic diagram for emulating TLP tester

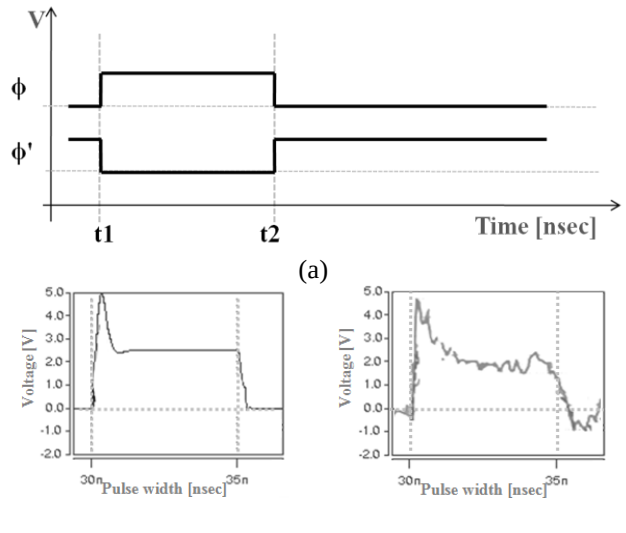


Figure 3. (a) The timing diagram to generate TLP pulse (Pulse width = t2-t1), (b) the simulated results, and (c) the measured results

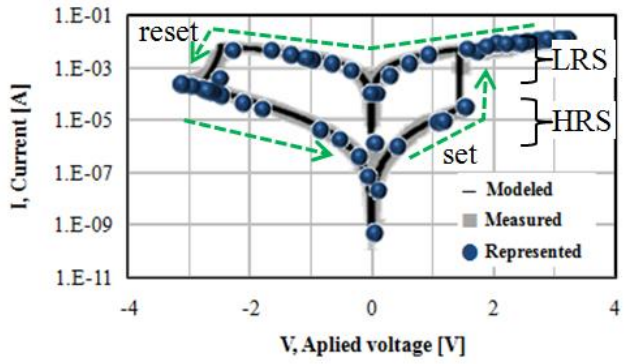


Figure 4. The I-V curves of a ReRAM cell: modeled (Solid line) and measured (Gray bold line) results of the prior work, and represented (Circles) result of this work

2. 1 Emulation of an ESD condition using SPICE simulation

In order to verify the correct operation state of the elements and the circuit in an ESD event conditions, the reproduction of ESD conditions through simulation is very convenient and important. The research on the emulation of the ESD event was presented. [5] In this work, the simulation environment for the emulation of the applied pulse wave in EDS event is build to examine the voltage level of the each node of the circuit within the ReRAM device by a injected ESD surge.

Figure 2 show the basic structure related to the generation of a pulse wave in TLP tester used for the ESD test and the reproduced schematic diagram through the faithful modeling of the TLP structure. Through the control of the two switches in the circuit, the Transmission line (T-line) connected the high voltage node (hv) for a period of time generates a pulse wave, and the pulse wave is transmitted to the DUT (Device under test).

In figure 3, a timing diagram of the two switches associated with the T-line and the simulated result of pulse wave are shown. Also, through the comparison of the measured data in the actual TLP equipment, it can be confirmed that both the rising time and the width of pulse is in good agreement with the simulated result.

2. 2 Verification of the Modeling result of RERAM

The research on the modeling of the ReRAM Cell was presented in [2]. Figure 4 shows measured and modeled I-V curves of the ReRAM cell in the prior work. When a voltage over +1.4V as a set voltage is applied across the ReRAM cell having the initial state of high resistive state (HRS), The resistive state of the ReRAM is changed to a low resistive state (LRS). In this state, as long as the voltage is not applied more than -2.5V as the reset voltage, ReRAM maintains the LRS state. But, if the voltage is reached the reset voltage, the resistive state of ReRAM is changed back to the HRS. The reproducing results of the ReRAM modeling in this work are added in Figure 4. The reproduced I-V curve shows exactly the transitions of the resistive state at set voltage of 1.4V and reset voltage of -2.5V..

2. 3 Circuit implementation and verification of the Proposed circuit for ESD detection and storage

Figure 5 shows the implemented circuit with ReRAM cell for the detection an ESD event and storage the ESD information. The proposed circuit is composed of a storage part with ReRAM cell, a detection part with RC network and the control block for read / reset operation of the ReRAM. The initial state of the ReRAM cell is set to HRS state. Another resistance (R2) in the circuit is carefully set not to reach the set level of the ReRAM cell during normal operation. The signal "ϕ" for the reset control of ReRAM is maintaned always low state.

When the ESD event is occurred and the voltage of the power line (VDD) in system is changed to high by the ESD surge voltage, the gate node of N1 transistor connected the RC-network is high, and N1 transistor is turned on due to

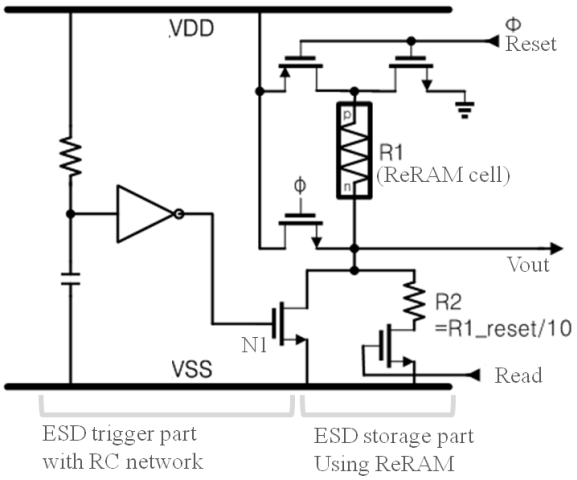


Figure 5. The proposed circuit diagram for the detection and the storage of ESD information

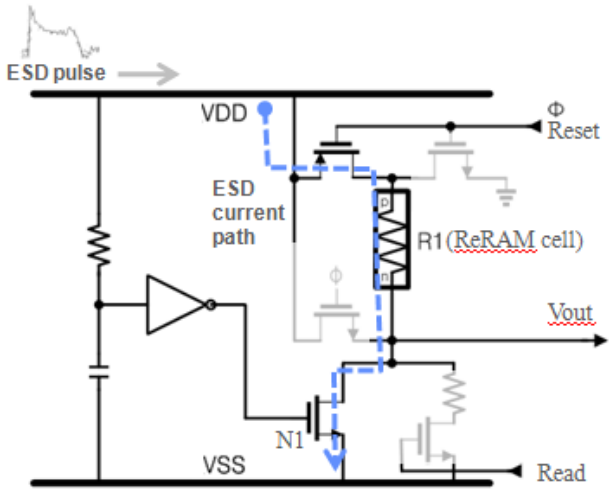
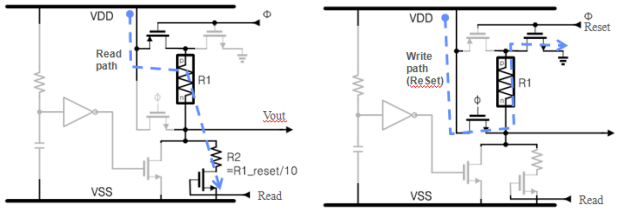


Figure 6. The circuit operation and ESD current path under EDS event



(a) (b)

Figure 7. (a) The path for read operation, and (b) the path for the reset operation of the ReRAM

the triggering operation of the RC-network, and the current path is formed through the ReRAM cell (R1). If the voltage level of VDD is over the set level, the ReRAM cell is changed to LRS state. This procedure is shown in Figure 6. The changed value of ReRAM during the ESD event still remains in Power-off condition. The simulation result of the ReRAM resistance by ESD is presented in Table 1.

Figure 7 show the read operation for reading the resistance value of the ReRAM cell and the reset operation to change the resistive state to HRS after the ESD event is

TABLE I
The Summary of simulation Results

Category		Simualted result	
		Before ESD	After ESD
ReRAM	State	HRS	LRS
	Resistance	161 KOhm	250 Ohm
Vout (@ VDD=2.8V)		2.54V	0.04V
Converted digital Code		0000	1111

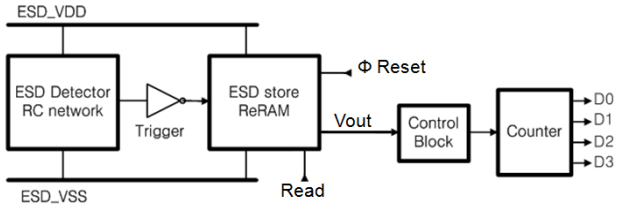


Figure 8. The block diagram of decoder circuit for the post processing of the stored ESD information

finished. When VDD is the voltage level of normal operation and the Read signal is high, the current path from VDD to VSS through R1 and R2 is formed. At this time, the level of the Vout node is determined by the resistance ratio in series connection of R1 and R2. The value of the Vout node which is changed by a resistance value of R1 as ReRAM may determine if an ESD event has occurred. The simulation result of the Vout node voltage by ESD is presented in Table 1.

After the read operation is finished, the reset operation is executed for the next ESD event. When the reset signal "ϕ" is high, The VDD level is to be applied in the reverse direction to the ReRAM, and the voltage across ReRAM is reached the reset level to be changed to the state HRS.

2. 4 Consideration to use the information stored in the ReRAM

Finally, the diagram of a decoder circuit for converting the detected ESD information into a digital code is introduced in Figure 8. When the read signal is high, the voltage of the Vout node is passed the next decoder block converting the voltage value into the digital code value. An example of decoding is presented in Table I. The system designed to always detect can execute a prepared actions to prevent the soft error due to a malfunction.

3. Conclusion

In this work, we proposed the ESD detection and storage circuit using ReRAM cell that operate regardless power condition. It was verified that the resistance of the ReRAM

Changes as expected under the ESD event regardless of power, and the read and reset operation of the proposed circuit work very well. For the verification of the proposed circuit, the SPICE simulation environment of the ESD emulation was build, and the modeling of the ReRAM was secured. Also through converting the stored information into the digital code, it is introduced that the malfunction due to ESD soft error may be prevented. It is expected that this work will be helpful for future studies for the ESD protection of the ReRAM itself as well as the soft error protection of the various mobile devices under set level ESD.

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