Design of an ADALINE Adaptive Filter Based Noise Cancellation Based on Fine-grained Pipelines

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Abstract: In this paper, a design of an ADALINE adaptive filter based noise cancellation based on fine-grained pipelines is presented. The circuit is implemented from 32-bit floating-point arithmetic function units which are partitioned into proper fine-grained pipeline stages. Fine-grained pipeline resource-sharing is performed to minimize the circuit size. The ADALINE adaptive filter is implemented on an FPGA (Xilinx SPARTAN-3 XC3S400) to perform power line noise reduction. The performance is also evaluated. The proposed fine-grained pipelines implementation archived much higher throughput than the implementation on a commercial DSP chip, and two times higher than the normal pipeline implementation.

Keywords: fine-grained pipeline, ADALINE, noise cancellation, FPGA

1. Introduction

Noise cancellation is necessary to obtain clear signals for digital signal processing (DSP) systems. An adaptive linear neural network (ADALINE) filter has been effectively used to reduce power line noise [2] and adaptive controls [3]. However, the noise cancellation circuit may dominate the whole circuit and degrade the DSP system performance [4]. Therefore, it is necessary to design a high throughput noise cancellation circuit so that the DSP system can analyze the input signals within desired time-constraints.

Fine-grained pipelines have potential to increasing the throughput [7],[8], [5], [9]. However, the circuit implementation often suffer from the pipeline stage partitioning problem and area insufficient. The fine-grained pipeline is adopted to increase the throughput rate of the feedforward circuit of an adaptive Neuro-fuzzy circuit using the GALS (globally-asynchronous-locally-synchronous) architecture [1]. The circuit was partitioned into three global stages communicating in asynchronous style. Each global stage has three sub-stages communicating in synchronous style. In [6], a high throughput power-aware FIR filter based on pipelining multipliers and adders can achieve very high throughput. However, the arithmetic function units such as multipliers or adders are not pipelined module and this GALS architecture is not suitable for the ADALINE adaptive filter.

In this paper, we propose an optimized fine-grained pipeline design for an ADALINE adaptive filter based noise cancellation. The 32-bit floating-point arithmetic function units are partitioned into proper stages. The circuits implemented from these partitioned units are called fine-grained pipelines. Fine-grained pipeline resource-sharing is performed to minimize the circuit size. The ADALINE adaptive filter is implemented on an FPGA (Xilinx SPARTAN-3 XC3S400 [11]) to perform power line noise reduction. The better performance is also evaluated compared to a commercial DSP chip and the normal pipeline implementation.

2. Noise cancellation

Fig. 1 shows a noise reduction system used in this paper. The measurable signal ($s + n_0$) is composed of signal (s) plus noise (n_0). There is no need for external reference signal in the system because the delay version of measurable signal (P) is used as a reference. The output signal from the adaptive ADALINE filter (a) is an estimation of the noise signal n_0. The error signal (e) is used for adjusting weight (w) and bias (b) of the adaptive filter based on Widrow-Hoff learning rule or least mean square (LMS) algorithm [10]. When the algorithm converges, we can reduce the noise signal from the measurable signal, i.e., $a \cong n_0$ and $e \cong s$. This algorithm can work well when the noise signal is periodic and the signal is aperiodic. Fig. 2 shows a flow chart of noise reduction system implementation based on the adaptive ADALINE filter and LMS algorithm.

In this paper, parameters used in the design of the ADALINE adaptive filter are as follows: number of tapped delay line = 8, delay = 10 and learning rate (α) = 0.005. Therefore, the functions of a, e, w, and b are as follows.

$$a(k) = w_1 p_1(k) + w_2 p_2(k) + ... + w_9 p_9(k) + b \quad (1)$$

$$e(k) = s(k) + n_0(k) - a(k) \quad (2)$$

$$w_i(k+1) = w_i(k) + 2\alpha p_i(k) e(k), i = 1, 2, ..., 9 \quad (3)$$

$$b(k+1) = b(k) + 2\alpha e(k) \quad (4)$$

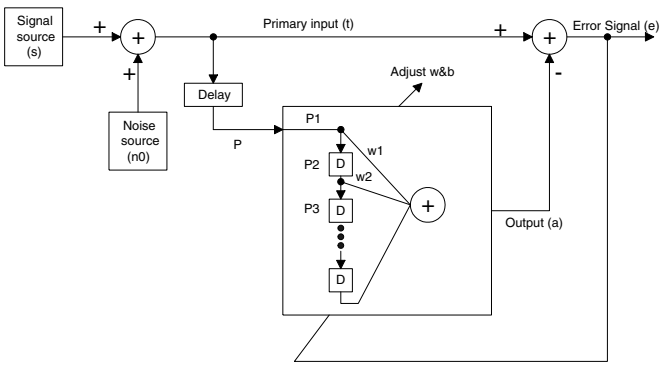


Figure 1. An ADALINE adaptive filter based noise cancellation circuit.

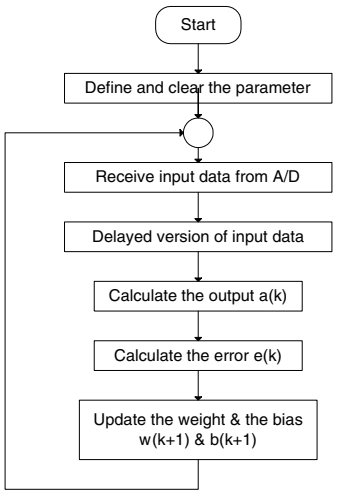


Figure 2. Flow chart of noise reduction system implementation based on ADALINE adaptive filter and LMS algorithm.

3. Fine-grained pipeline design

The circuit model proposed in this work is shown in Fig.3. An arithmetic function unit (such as a multiplier, an adder) is partitioned into proper stages. The arithmetic function unit shown in Fig.3(a) may be partitioned into fine-grained pipeline as in Fig.3(b). To obtain the optimum throughput, all partitioned stages should be balanced. If the balanced partitioning cannot be obtained, the longest pipeline stage delay must become the pipeline clock speed. In this paper, the 32-bit floating point multipliers are 3-stage fine-grained pipelines, and the 32-bit floating point adders are 4-stage fine-grained pipelines. These modules are used to implement the DSP functions which can be represented in DFG (Data Flow Graph). For example, the DFGs of equation (1) and (3)+(4) are shown in Fig.4(a) and 4(b), respectively.

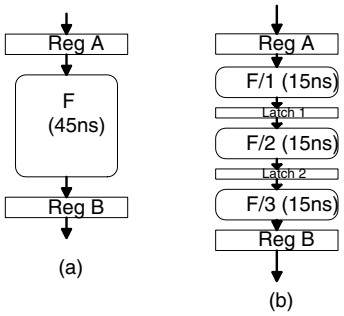
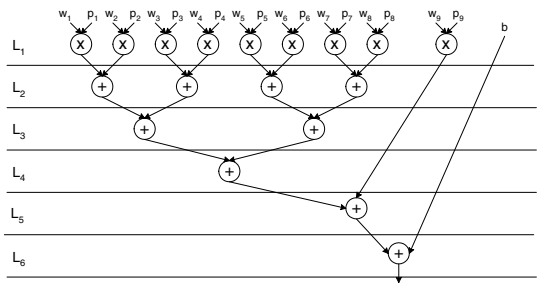
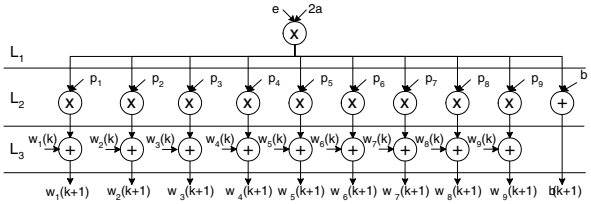


Figure 3. A fine-grained pipeline: a functional circuit (a), a fine-grained pipeline circuit (b).

In this paper, a fine-grained pipeline resource-sharing is used to minimized the circuit size. Fig. 5 shows the resource-sharing of the DFG of Fig. 4(a). Note only some parts are shown because of paper space. After the 1st stage of multiplier M1 has completed, it is available to execute the next data. Similarly, the other pipeline stages act in the same manner.



(a) an 8-tapped delay ADALINE DFG



(b) a weight and bias adjustment DFG

Figure 4. Data flow graphs.

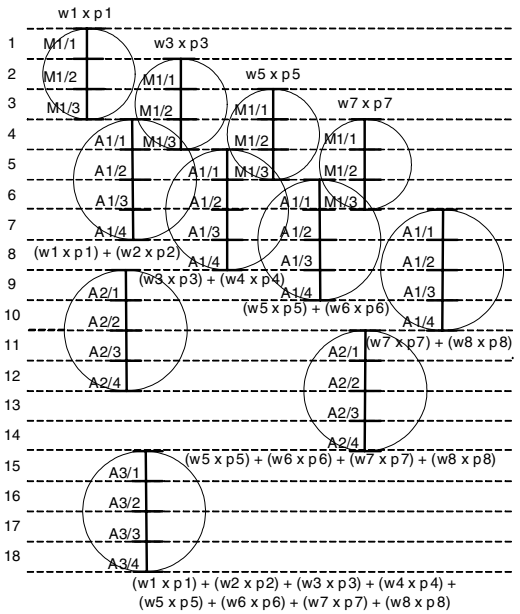


Figure 5. Resource-sharing in fine-grained pipelines.

The resource sharing between data dependence operations is not allowed, because the pipeline parallel property may lose and the controller is too complicated. From a given DFG, the operations are assigned into the corresponding $level$, i.e. the order from the input data. The resource sharing is allowed only for the operations in the same level. For example, the multiply operations in level L_1 can share the same fine-grained pipeline multiplier. In contrast, the addition operations in level L_2 are not allowed to use the same fine-grained pipeline adder as the addition operations in level L_3 because of the data dependence.

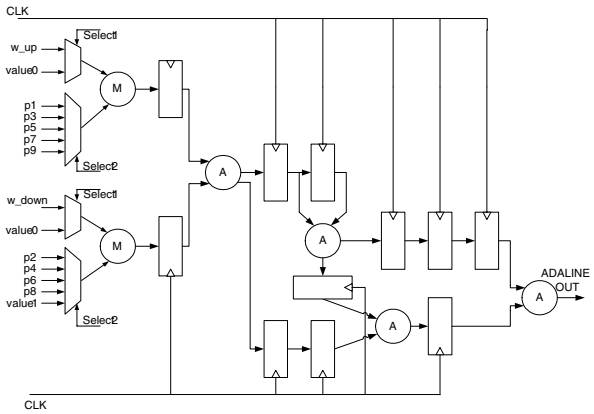


Figure 6. The synthesized 8-tapped delay ADALINE circuit.

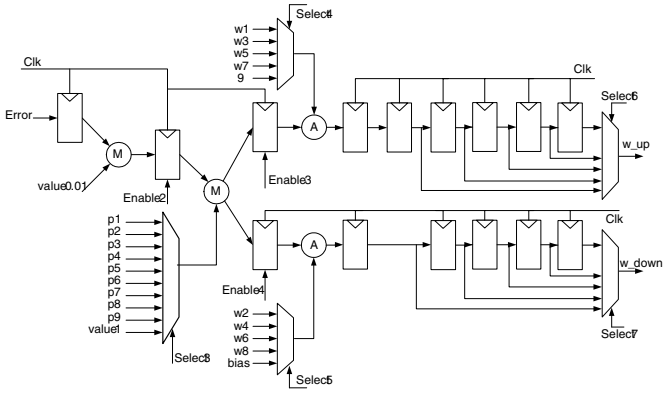


Figure 7. The synthesized weight and bias adjustment circuit.

The synthesized circuits are as follows. Fig.6 shows the synthesized 8-tapped delay ADALINE circuit, i.e. the implementation of equation (1). The sharing resources are two multipliers and four adders. Fig.7 shows the synthesized weight and bias adjustment circuit, i.e. the implementation of equations (3) and (4). This circuit uses two multipliers and two adders. Fig.8 shows the top level of the ADALINE adaptive filter based noise cancellation circuit. The multiplexor select signals and the register enable signals are generated from the control circuit at the proper time to allow the circuit work correctly. The control circuit is the FSM (Finite State Machine) in Moore machine format to keep the control signals stable throughout the corresponding control steps.

4. Evaluation Results

4.1 Power line noise reduction

The proposed ADALINE adaptive filter based noise cancellation based on fine-grained pipelines has been implemented on an FPGA (Xilinx SPARTAN-3 XC3S400 [11]) and tested. Fig. 9 (Top Left) shows an example of SEMG (surface electromyography) waveform from electrode sites before the reduction in power line noise. Fig. 9 (Top Right) shows the corresponding spectrum of time waveform in the left column. Please note that the 50-Hz power line noise and its odd harmonics, i.e., 150, 250, 350, and 450 Hz are clearly observed. The waveform of SEMG after the reduction in power line noise and its spectrum are shown in Fig. 9 (Bottom Row). It has been shown that the 50-Hz power line noise and its odd harmonics are effectively suppressed by the ADALINE adaptive filter.

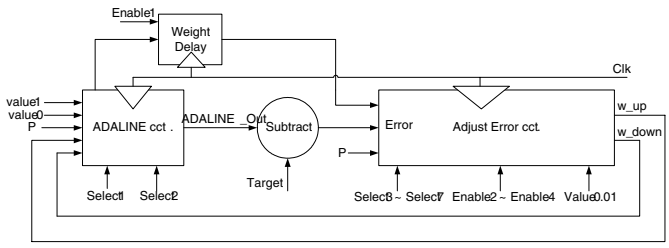


Figure 8. The synthesized ADALINE adaptive filter circuit.

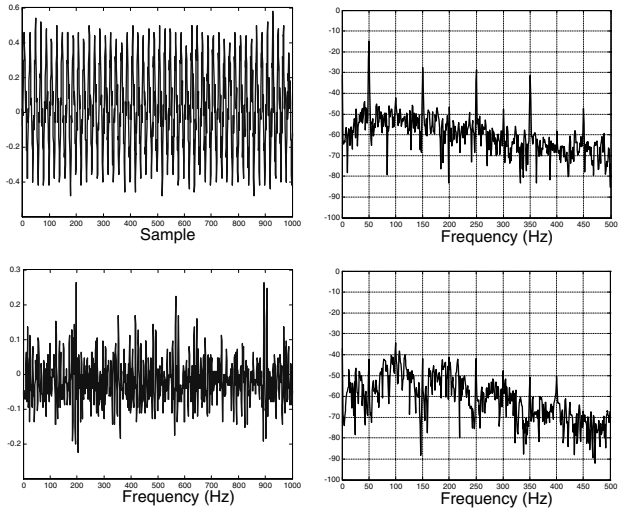


Figure 9. Top Left: SEMG signal before the reduction in power line noise. Bottom Left: SEMG signal after the reduction in power line noise. The right column is corresponding spectra of time waveforms in the left column.

4.2 Performance results

To evaluate the proposed method, the noise cancellation circuit of Fig.1 was implemented on an FPGA (Xilinx SPARTAN-3 XC3S400 [11]) in two implementations: a normal pipeline implementation (arithmetic function units are not pipelined), and the proposed fine-grained pipeline implementation. Table 1 shows the evaluation results compared to the implementation on a DSP chip (TMS320VC5509A). The 1st column shows the implementation style. The 2nd column shows operation clock speed. The TMS320VC5509A ran at 200 MHz. The normal pipeline clock speed was 20 MHz generated from the Xilinx DCM (Digital Clock Manager) v8.1i [11]. Actually, the synthesized clock speed was

Table 1. Performance comparison on various solutions

Implementations	Clock speed (MHz)	Throughput (Samples/sec)
DSK TMS320VC5509A [2]	200	245,908.04
FPGA XC3S400 (normal)	20	2,000,000.00
FPGA XC3S400 (fine-grained)	40	4,000,000.00

20.5086 MHz, but the DCM cannot exactly generate this speed. Similarly, the fine-grained pipeline clock speed was 40 MHz whose synthesized clock speed of 41.44 MHz. The last column of Table 1 shows the throughput of each implementation. Obviously, the implementations on the FPGA archived much higher throughput than the implementation on the DSP chip. The proposed fine-grained pipeline implementation archived two times higher throughput than the normal pipeline implementation.

5. Summary

A design of an ADALINE adaptive filter based noise cancellation based on fine-grained pipelines has been presented. The circuit was implemented from 32-bit floating-point arithmetic function units partitioned into proper fine-grained pipeline stages, i.e. 3-stage fine-grained pipeline multipliers and 4-stage fine-grained pipeline adders. Fine-grained pipeline resource-sharing was performed to minimize the circuit size. The proposed ADALINE adaptive filter was implemented on an FPGA (Xilinx SPARTAN-3 XC3S400) to perform power line noise reduction. The better performance was also evaluated compared to a commercial DSP chip and the normal pipeline implementation.

Acknowledgements

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