A Method to Improve Linearity of a Variable Operating Range Transconductor

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Abstract: A transconductor using bias offset technique is known as a linear MOS transconductor. The linearity is deteriorated by nonideal factors. Major deterioration is caused by mobility degradation from an effect of vertical field. This paper proposes a linearization technique of the MOS transconductor following change of operating range. This technique improves the linearity of transconductance characteristic by adding two MOS-FETs operating as resistors and a source follower to the conventional circuit.

1. Introduction

A transconductor is a fundamental building block for analog signal processing circuits, such as filters, multipliers and oscillators. The transfer characteristic is desired to be linear. However, the linearity is deteriorated by nonideal factors. Major deterioration is caused by mobility degradation from an effect of vertical field. Several methods to improve the linearity have been proposed[1]–[4]. This paper proposes a linearization technique of the MOS transconductor following change of operating range and gain. The modified conventional circuits are based on the bias-offset transconductor[5], which is shown in Fig. 1. This technique improves the linearity of transconductance characteristic by adding two MOS transistors operating as resistors and a level shift circuit to the conventional circuit.

2. Conventional Circuit

Figure 1 shows the conventional circuit configuration of bias-offset transconductor[5]. Assuming that the drain current of an MOS transistor obeys the square-law characteristic, the drain currents of M1-M4 are expressed as

$$\begin{cases} I_{D1} = K_N(V_L - V_S - V_{TN})^2 \\ I_{D3} = K_N(V_R - V_S - V_{TN})^2 \\ I_{D2} = K_N(V_L - V_B - V_S - V_{TN})^2 \\ I_{D4} = K_N(V_R - V_B - V_S - V_{TN})^2 \end{cases} \quad (1)$$

where K_N is the transconductance factor, V_{TN} is the threshold voltage, V_S is common-source voltage of M1-

M4, respectively. Solving Eq.(1), the common-source voltage, V_S are eliminated. The output current I_{OUT} is expressed as

$$I_{OUT} = (I_{D1} - I_{D3}) - (I_{D2} - I_{D4}). \quad (2)$$

Assuming that the input voltages are fully differential signals, input voltage V_{IN} is expressed as

$$\begin{cases} V_{IN} = V_L - V_R \\ V_L + V_R = 0. \end{cases} \quad (3)$$

From Eq.(1)–(3), the output current I_{OUT} is expressed as

$$I_{OUT} = 2K_N V_B V_{IN}. \quad (4)$$

The transconductance G_m is expressed as

$$G_m = \frac{dI_{OUT}}{dV_{IN}} = 2K_N V_B. \quad (5)$$

From Eq.(5), assuming that the drain current of an MOS transistor obeys the square-law characteristic, the transfer characteristic G_m of the conventional transconductor is linear regardless of the input voltage V_{IN}. The conditions that four MOS transistors operate are given by

$$V_B + V_S + V_{TN} \leq \frac{V_{IN}}{2} \leq -V_B - V_S - V_{TN}. \quad (6)$$

From Eq.(6), the operation range of the transconductor is expressed as

$$|V_{IN}| \leq \frac{1}{2}\left(\sqrt{\frac{I_S}{2K_N} - \frac{3V_B^2}{4}} - \frac{V_B}{2} \right) \quad (7)$$

where I_S is the tail current. From Eq.(7), the operation range of the transconductor can be adjusted by the tail current I_S.

The output current I_{OUT} changes nonlinearly because of mobility degradation from vertical electric field. Considering mobility degradation, transconductance factor K_{eff} is given by

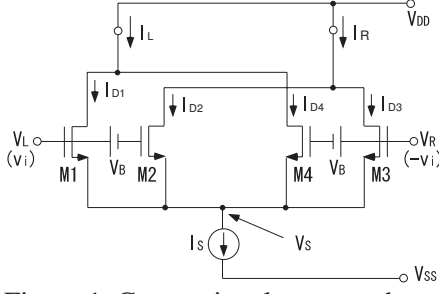$$K_{eff} = \frac{K_N}{1 + \theta(V_{GS} - V_{TN})} \quad (8)$$

Figure 1. Conventional transconductor

where θ is mobility degradation factor. Considering mobility degradation, the drain currents of M1-M4 are expressed as

$$\begin{cases} I_{D1} = \dfrac{K_N}{1 + \theta(V_L - V_S - V_{TN})}(V_L - V_S - V_{TN})^2 \\ I_{D3} = \dfrac{K_N}{1 + \theta(V_R - V_S - V_{TN})}(V_L - V_S - V_{TN})^2 \\ I_{D2} = \dfrac{K_N}{1 + \theta(V_L - V_B - V_S - V_{TN})}(V_L - V_B - V_S - V_{TN})^2 \\ I_{D4} = \dfrac{K_N}{1 + \theta(V_R - V_B - V_S - V_{TN})}(V_R - V_B - V_S - V_{TN})^2. \end{cases} \tag{9}$$

From Eqs.(3), (9), the output current I_{OUT} is expressed as

$$I_{OUT} = \frac{16K_N V_B((V_B + 2V_{ST}) - 2)\theta V_{IN}}{(A\theta + 2)(B\theta - 2)((A + 2V_B)\theta + 2)((B + 2V_B)\theta - 2)} \tag{10}$$

where V_{ST}, A, and B are given by

$$\begin{cases} V_{ST} = V_S + V_{TN} \\ A = V_{IN} - 2(V_S + V_{TN}) \\ B = V_{IN} + 2(V_S + V_{TN}). \end{cases} \tag{11}$$

Differentiating I_{OUT} with respect to V_{IN}, we obtain transconductance G_m. Figure 2 illustrates the numerical simulation results of the transconductance simulated considering the effect of mobility degradation and ideal one for $V_B = 0.1$[V], $I_S = 100[\mu A]$, $\theta = 0.197$. This figure shows that Linearity of transfer characteristics is deteriorated by mobility degradation.

3. Transfer Characteristic

Figure 3 shows the circuit configuration of the proposed circuit. The transfer characteristic is adjusted by resistance of M5 and M6 operating as resistors. Resistances of M5 and M6 are tuned by V_{CS} which is the voltage difference between V_S and V_C. The optimal condition for V_{CS} is obtained by the maximally flat approximation[8]. This condition is satisfied by M7, which is a source follower.
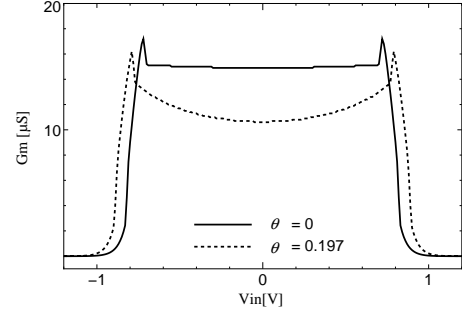

Figure 2. Simulation results of transconductance characteristics considering only mobility degradation
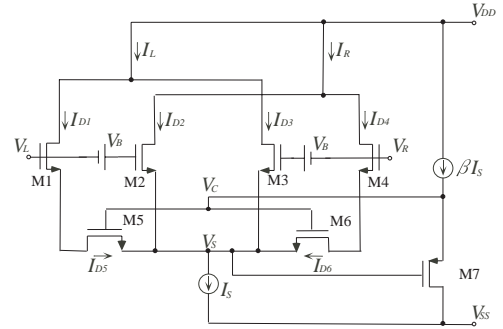

Figure 3. Proposed transconductor

3.1 Output Current

Because M5 and M6 are operating as resistors, the drain currents are expressed as

$$I_D = 2K_N(V_{CS} - V_{TN} - \frac{V_{DS}}{2})V_{DS}. \tag{12}$$

The reciprocal of the value of differentiated Eq.(12) with respect to V_{IN} is the resistance of M5 and M6. The resistance R is expressed as

$$R = \frac{1}{2\alpha K_N(V_{CS} - V_{TN} - \dfrac{V_{DS}}{2}) - \alpha K_N V_{DS}} \tag{13}$$

where α is aspect ratio of M5 and M6. From Eq.(13), the resistance of M5 and M6 can be adjusted by V_{CS}. Assuming that M5 and M6 are the resistors, the drain currents of M1-M4 are expressed as

$$\begin{cases} I_{D1} = \dfrac{K_N}{1 + \theta(V_L - RI_{D1} - V_{ST})}(V_L + RI_{D1} - V_{ST})^2 \\ I_{D3} = \dfrac{K_N}{1 + \theta(V_R - RI_{D3} - V_{ST})}(V_R + RI_{D3} - V_{ST})^2 \\ I_{D2} = \dfrac{K_N}{1 + \theta(V_L + V_B - V_{ST})}(V_L + V_B - V_{ST})^2 \\ I_{D4} = \dfrac{K_N}{1 + \theta(V_R + V_B - V_{ST})}(V_R + V_B - V_{ST})^2. \end{cases} \tag{14}$$

Table 1. Optimum values of $R\ [\Omega]$

V_B I_S	$50\mu A$	$100\mu A$	$150\mu A$	$200\mu A$
0.1 V	381	284	238	210
0.2 V	682	552	445	396
0.3 V	940	732	630	556
0.4 V	1178	924	801	723

Table 2. Optimum values of β

V_B I_S	$50\mu A$	$100\mu A$	$150\mu A$	$200\mu A$
0.1 V	9.178	10.82	11.49	11.84
0.2 V	0.990	1.660	1.981	2.170
0.3 V	0.187	0.396	0.572	0.691
0.4 V	0.001	0.051	0.293	0.273

The output current I_{OUT} of the proposed circuit is expressed as

$$I_{OUT} = (I_{D3} - I_{D1}) - (I_{D4} - I_{D2}). \qquad (15)$$

From Eqs.(3), (14), and (15), the output current I_{OUT} is expressed as

$$I_{OUT} = \frac{1}{4(K_N R + \theta)} \left[\left(\frac{4K_N^2 R}{\theta} - \frac{2\theta}{R} \right.\right.$$

$$+ \frac{16K_N(K_N + \theta)}{\theta(A\theta - 2V_B\theta - 2)(B\theta + 2V_B\theta + 2)} \Bigg) V_{IN}$$

$$+ \frac{1}{R} \Big(\sqrt{(B\theta + 2)^2 + 8AK_N R}$$

$$\left.\left. - \sqrt{(A\theta - 2)^2 - 8AK_N R} \Big) \right] \right.$$

$$(16)$$

where V_{ST}, A and B are given by Eq.(11). Differentiating Eq.(16) with respect to V_{IN} gives transconductance G_m.

3.2 Linearization

The optimal linearization condition for R is obtained by the maximally flat approximation[8]. Using Maclaurin expansion, G_m is expressed as

$$G_m(V_{IN}) = \\ G_m(0) + \frac{G'_m(0)}{1!}V_{IN} + \frac{G''_m(0)}{2!}V_{IN}^2 + \frac{G_m^{(3)}(0)}{3!}V_{IN}^3 + \cdots .$$

$$(17)$$

Because G_m is an odd function, Eq.(17) is expressed as

$$G_m(V_{IN}) = G_m(0) + \frac{G''_m(0)}{2!}V_{IN}^2 + \frac{G_m^{(4)}(0)}{4!}V_{IN}^4 \cdots . \quad (18)$$

In this case, the proposed circuit has only one parameter R for linearization. Thus the maximally flat condition is given by
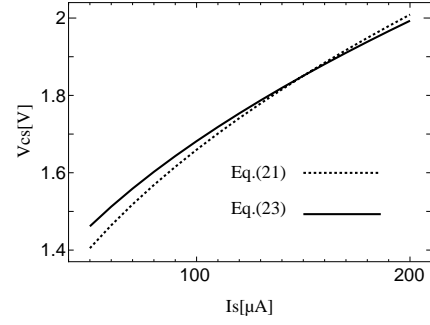
$$G''_m(0) = 0. \qquad (19)$$

Solving Eq.(19) for R, the optimum values of R are obtained. Table 1 shows optimum values of R for various V_B and I_S. V_{DS} of M5 is expressed as

$$V_{DS} = I_{D1}R. \qquad (20)$$

Figure 4. V_{CS} characteristics for Eqs.(21), (23)

Eliminating V_{DS} from Eqs.(13), (20), the condition of V_{CS} for linearization is given by

$$V_{CS} = \frac{1}{2\alpha K_N R(K_N R + \theta)}$$

$$\times \Big(\theta + K_N R \Big(1 + \alpha \big(1 - (2K_N R + \theta)V_S + \theta V_T$$

$$- \sqrt{(V_{ST}\theta - 1)^2 - 4K_N R V_{ST}} \big) \Big) \Big)$$

$$(21)$$

where V_S is expressed as

$$V_S = \frac{-K_N V_B - 2K_N V_{TN} - \sqrt{I_S K_N - K^2 V_B^2}}{2K_N}.$$

$$(22)$$

Subsutituting the optimum R in Table 1 into Eq.(21), the linearization condition is obtained.

Eq.(21) is approximately realized by the source follower. The ratio of the bias current of the source follower to the tail current I_S is defined as β. The voltage of V_{CS} of the source follower is given by

$$V_{CS} = \sqrt{\frac{\beta}{K}}\sqrt{I_S} + V_{TN}. \qquad (23)$$

Figure 4 illustrates V_{CS} of Eqs.(21), (23). This figure shows that the source follower is valid to realize the optimal condition adopting an adequate value of β. Table 2 shows optimum values of β for various V_B and I_S for linearization.

Table 3. Transconductance error for $V_B=0.1$[V]

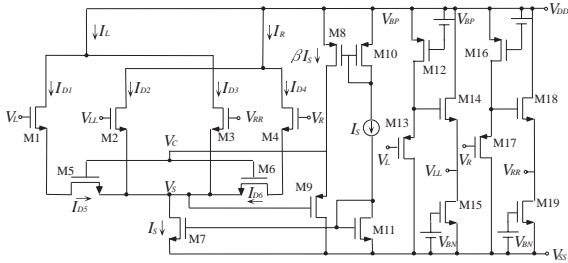| I_S	100 μA	150 μA	200 μA
Conventional	29.4 %	36.3 %	48.4 %
Proposed	9.52 %	11.2 %	12.1 %

Figure 5. Circuit configuration of proposed circuit

4. simulation

In order to confirm the validity of the proposed technique, SPICE simulation was carried out. The transconductance factors of nMOS and pMOS transistors for $W/L = 1$ are 177[μS/V] and 40.7[μS/V], respectively. The mobility degradation factors θ of nMOS and pMOS transistors are 0.1973 and 0.036, respectively. Figure 5 illustrates the circuit configuration for SPICE simulation. Figure 6 illustrates the transconductance characteristics for different tail currents. The transconductance errors for $V_B = 0.1$[V] are listed in Table 3. It should be noted that the proposed transconductor exhibit improved linearity for each condition.

Figure 7 illustrate the frequency characteristics. Comparing the simulation result of the conventional circuit and the proposed circuit, frequency characteristics are almost the same.
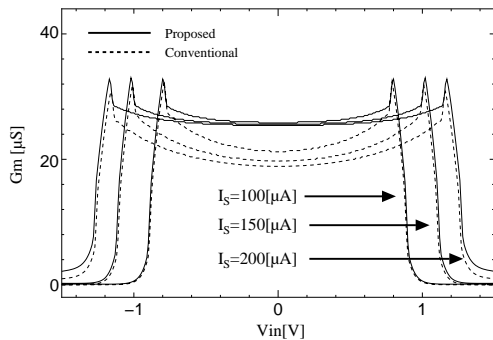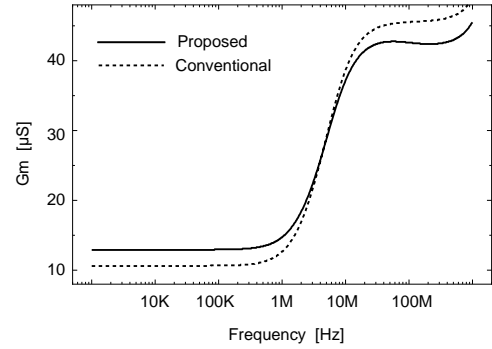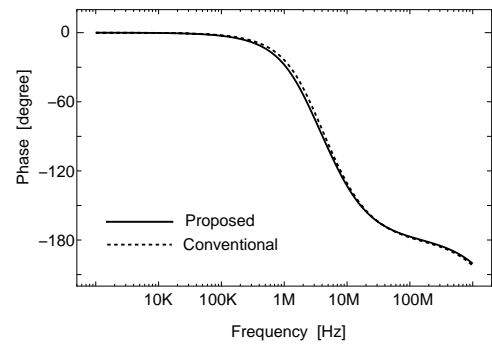

Figure 6. Transconductance characteristics of the proposed circuit

(a) G_m

(b) Phase

Figure 7. Frequency characteristics

5. Conclusion

This paper has proposed a new linear MOS transconductor based on the bias-offset transconductor for variable operating range. In order to confirm the validity of these methods, SPICE simulation was carried out. Simulation results show that the proposed circuits have good linearity for the variable operating ranges.

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