An improved bipolar multiplier using a high linear transconductors with wideband input

Sung-Ho Yun, Yun-Mi Na, and Hyeong-Woo Cha

School of Electronic Communication Eng., Cheongju University
36 Naedok-dong, Sangdang-gu, Chongju-shi, Chung-buk, 360-764, Korea,
Phone : +82-43-229-8441, Fax : +82-43-229-8432
E-mail : hwcha@cju.ac.kr

Abstract : A improved bipolar multiplier using a high linear transconductors with wide dynamic range for accuracy instrumentation system was designed. The multiplier consists of two high linear transconductors, a multiplier core, and a differential to single-ended converter. The transconductor has high linear and wide dynamic input range because of adaptive bias circuits. For the verification of the performance for the proposed multiplier, we simulated with the circuit of the commercial device of the AD534. The simulation result shows that the AD534 has dynamic range of ±10V and the proposed multiplier has ±13V at supply voltage ±15V, respectively. The linearity error of the proposed multiplier was five times smaller than that of the AD534. The power dissipation of the multipliers were the same.

1. Introduction

A multiplier is an essential device for analog computations, signal modulation and demodulation, and voltage controlled oscillators and filters. Conventionally, the bipolar multiplier consists of two voltages to current converter (linear transconductor), multiplier core, and a differential to single-ended converter. For wide dynamic range of the multiplier, the design of the high linear transconductor with a wide dynamic range is very important. The commercial multiplier devices of the AD534 and MC1595 used laser trimming or external accuracy resistors in order to get linearity and wide dynamic range [2-4]. In the case, the device had high cost and inconvenience for the applications.

In this paper, an improved bipolar multiplier using two high linear transconductors with wide dynamic range was designed. We introduce a principle for the proposed multiplier, and then discuss the results of simulation in next sections

2. Circuit descriptions

2-1 The commercial multiplier AD534

The circuit diagram of the AD534 is shown in Fig. 1[2]. The circuit consists of two transconductors, a multiplier core, and a differential to single-ended converter. The one transconductor composed with Q_1, Q_2, R_4, R_5, and R_8, the other Q_3, Q_4, R_6, R_7, and R_9. The multiplier core consists of $Q_5 \sim Q_{10}$ and the differential to single-ended converter consists of operational amplifier, Q_{16}, Q_{17}, $R_{15} \sim R_{17}$, and $R_{18} \sim R_{20}$.

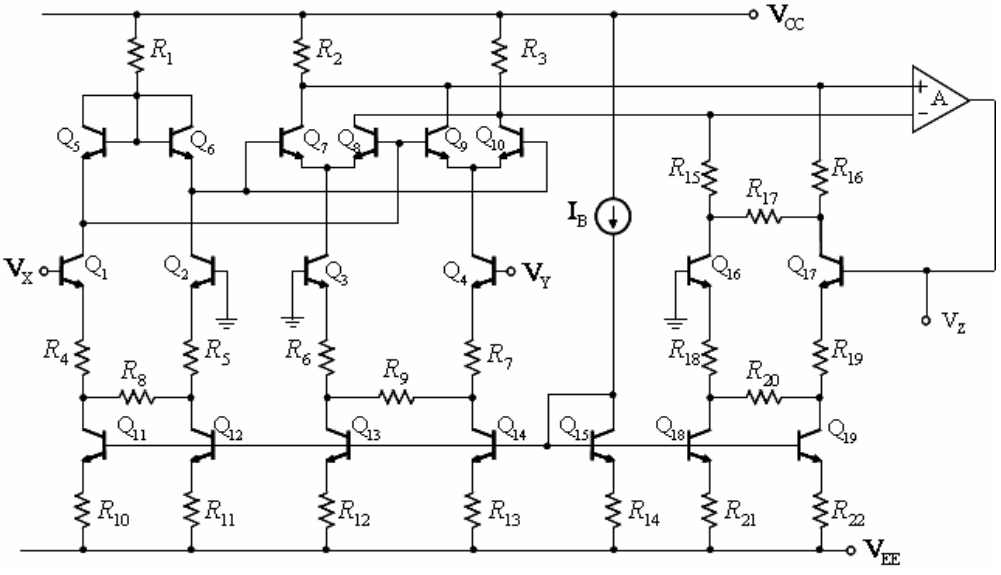

Fig. 1 Circuit diagram of the commercial multiplier AD534

The bias circuit composed with $Q_{11} \sim Q_{19}$, $R_{10} \sim R_{14}$, and R_{21}, R_{22}. The output voltage V_Z for V_X and V_Y of the AD534 can be written as follow [2] ;

$$V_Z = \frac{1}{I_{REF} R_8} \frac{2R_{15} + R_{17}}{R_{17}} V_X V_Y \qquad (1)$$

The AD534 completed monolithic chip exhibits a total error or less than ±0.5% of full scale over the entire operating temperature range, with a scale-factor temperature coefficient of + 75ppm/C. The nonlinearity errors are less than 0.15% of full scale. The circuit is designed to operate with ±15V supplies and ±10V input dynamic range [2].

2-2 A high linear transconductor with wideband input [1]

The complete circuit diagram of a high linear transconductor with wideband input is shown in Fig. 2. Since the base-emitter junctions of Q_{1B} and Q_{2B} are connected in parallel with those of Q_{1A} and Q_{2A}, respectively, we can write $i_{C1B} = i_{C1A} = i_{C1}$ and $i_{C2B} = i_{C2A} = i_{C2}$ under the assumption that four transistors are identical. To bias transistor Q_3 with collector current of Q_{1A}, the collector current i_{C1A} is reproduced at the emitter of Q_3 through the basic current formed by Q_7 and Q_8. The output current $i_O = i_{C1} - i_{C2}$ can be taken by connecting a pnp current mirror between the collector terminals of Q_{1B} and Q_{2B} and the positive power supply. The resultant output current will be given by $i_O = v_{IN} / R_E$ for linear range of $I_{EE} R_E$ [V]. The expansible range of the input dynamic $v_{IN}(DYM)$ is given by

$$V_{EE} - V_{sat}(I_{EE}) < v_{IN}(DYM) < V_{CC} - V_{BE3} - V_{sat}(i_{C1}) \qquad (2)$$

where $V_{sat}(I_{EE})$ and $V_{sat}(i_{C1})$ are saturation voltages for the output transistors of basic current mirrors realizing current sources I_{EE} and i_{C1}, respectively. The equation (2) notices that the input dynamic range can be widened for low supply voltage V_{EE}.

2-3 Design of the improved multiplier

The circuit diagram of the proposed multiplier is shown in Fig. 3. The circuit consists of two proposed transconductors shown in Fig. 2, a multiplier core, and a differential to single-ended converter.

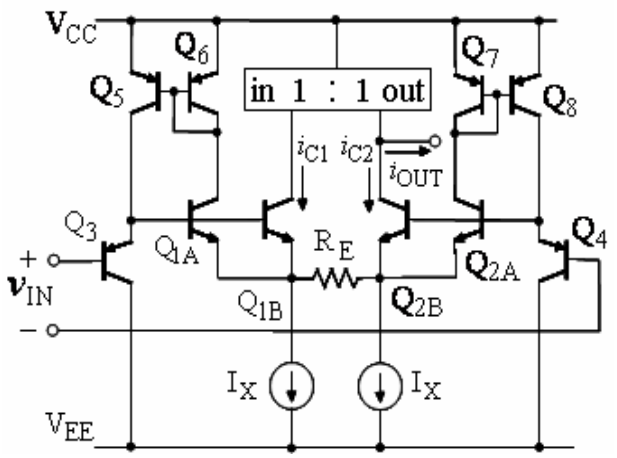

Fig. 2 A high linear transconductor with wideband input[1]

The one transconductor composed with $Q_1 \sim Q_{12}$ and R_1, the other $Q_{13} \sim Q_{24}$ and R_2. The multiplier core consists of $Q_{25} \sim Q_{30}$ and $R_3 \sim R_5$ The differential to single-ended converter consists of operational amplifier, $Q_{33} \sim Q_{37}$, and $R_6 \sim R_{14}$. The bias circuit of the transconductors composed with I_{B2} and $Q_{31} \sim Q_{32}$. This circuit has same as construction with AD534 but the main block of linear transconductors was different configuration than AD534.

The principle of the operating also was same as AD534. Therefore, the output voltage V_Z for the input V_X and V_Y shown in Fig. 3 can be written as follow;

$$V_Z = \frac{1}{I_{B2} R_1} \frac{2R_6 + R_8}{R_8} V_X V_Y \qquad (3)$$

3. Simulation results and Discussion

The operation of the proposed multiplier shown in Fig. 3 was simulated by using PSPICE with commercial transistor mode parameters of Q2N3404(*npn*) and Q2N3406(*pnp*). The supply voltage V_{CC}= 15V, V_{EE}= −15V, I_B=I_{B1}=300μA , I_{B2}=350μA . The amplifier A was LM741. For the verification of the performance for the proposed multiplier, we simulated with the circuits of the commercial device of AD534.

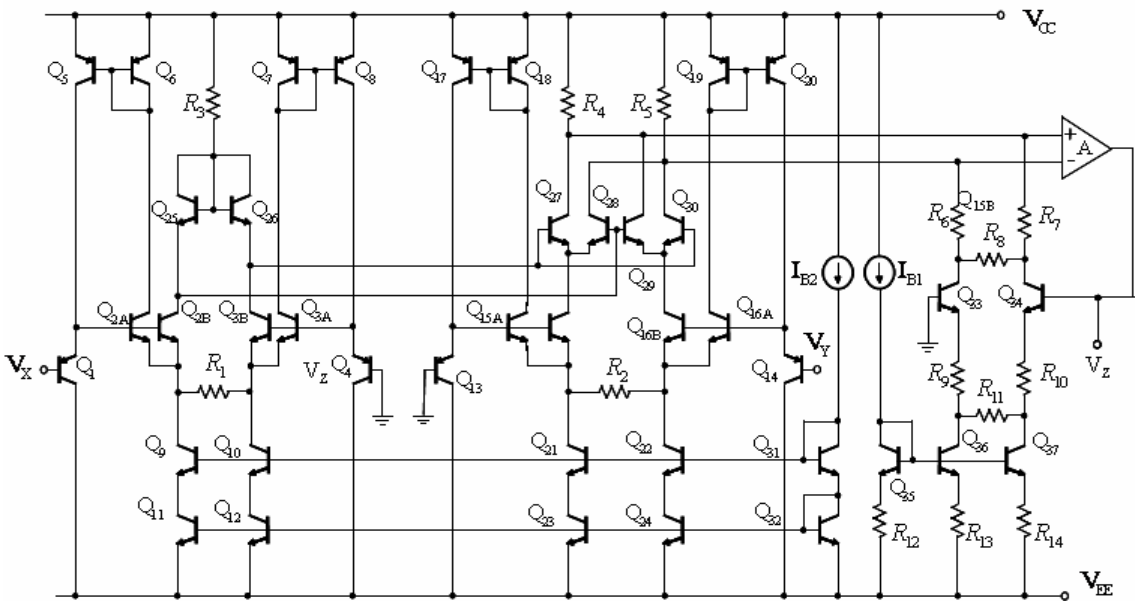

Fig. 3 Circuit diagram of the proposed multiplier using the transconductors

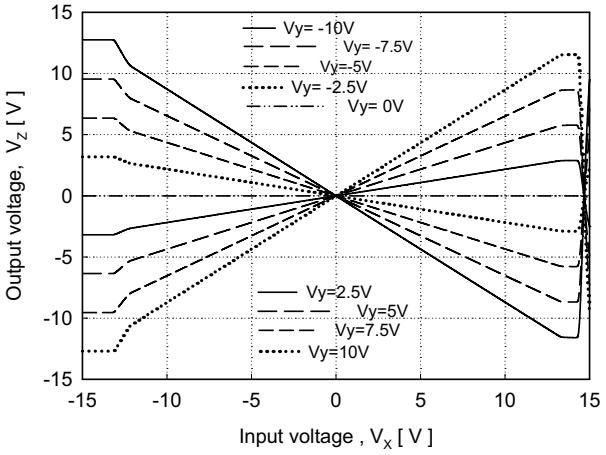

Fig. 4 Multiplication characteristics of Vx versus Vy shown in Fig. 1

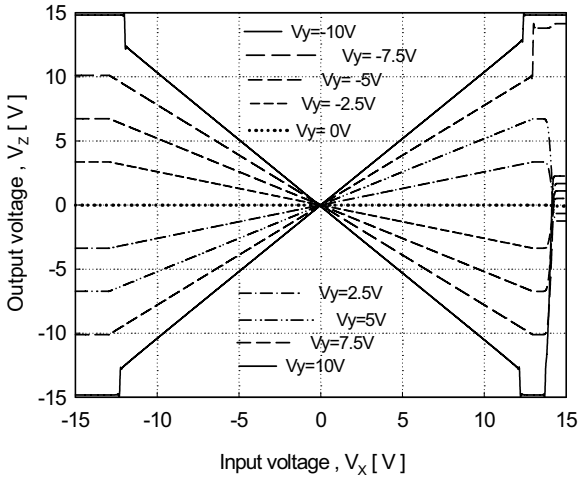

Fig. 5 Multiplication characteristics of Vx versus Vy shown in Fig. 3

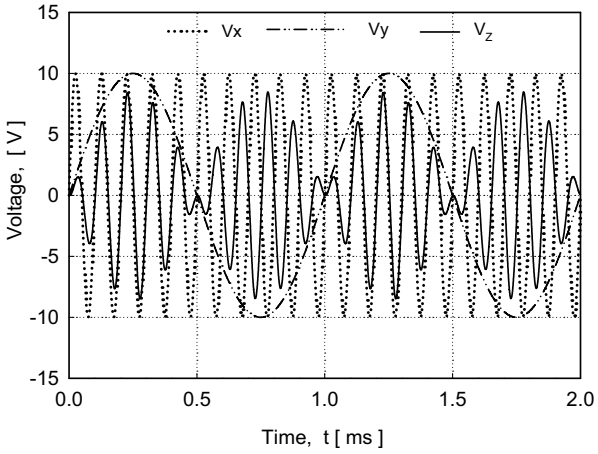

Fig. 6 Amplitude modulation characteristics shown in Fig. 1

Fig. 4 shows the multiplication characteristics of input voltage V_X versus output V_Z at input voltage V_Y =−10V~10V shown in Fig. 1. It notices that the linearity was good the input voltage range −10V to 10V.

Fig. 5 shows the multiplication characteristics of input voltage V_X versus output V_Z at input voltage V_Y =−13V~13V for the proposed circuit shown in Fig. 3. It notices that the linearity was good for the input voltage range -13V to 13V. The linearity error of the proposed multiplier was five times smaller than that of the AD534.

The amplitude modulation (AM) characteristics of the AD534 for $V_X = 10\sin 2\pi 1kt$ [V], $V_Y = 10\sin 2\pi 10kt$ [V] shows in Fig. 6. It notices that the magnitude signal of AM 80% for the ideal value.

The amplitude modulation (AM) characteristics of the proposed multiplier for the same condition shows in Fig. 7.

It notices that the magnitude signal of AM 100% for the ideal value.

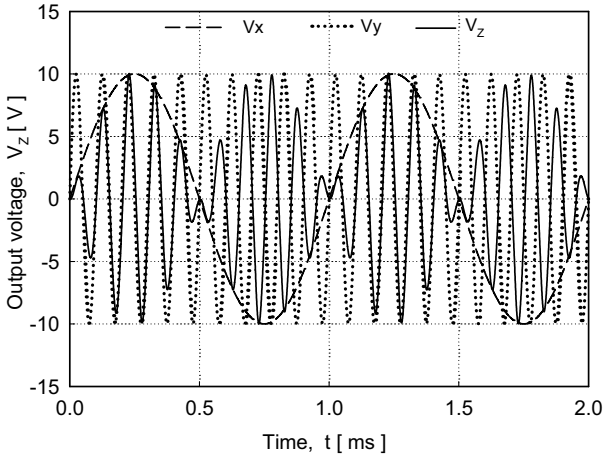

Fig. 7 Amplitude modulation characteristics shown in Fig. 3

4. Conclusions and future subject

An improved bipolar multiplier using a high linear transconductors with wide dynamic range for accuracy instrumentation system was presented. Simulation has demonstrated that the circuit has good characteristics of linearity and multiplication. Therefore, the proposed multiplier will be useful for building block of accuracy instrumentation measurement and communication systems. Now, we optimize the circuit of the proposed multiplier using fabrication model parameters. In the future, we will fabricate chip by bipolar process.

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5. References

[1] W.-S. Chung, H.-W. Cha, and S.-H. Son, "A low-voltage low-power bipolar transconductor with high-linearity," IEICE Trans. Fundamentals, vol. E88-A, no. 1, pp. 384-386, January 2005

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[4] Data sheet MC1595, Motorola