Parallel Sphere Decoder Architecture for MIMO System

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Abstract: Since Schnorr - Euchner Sphere Decoding (SE-SD) does not guarantee a fixed throughput, the searching cycles of SE-SD should be limited for the practical implementation. Given SE-SD with runtime constraint causes degradation in performance due to the variance of searching cycles, an enhanced SE-SD architecture with a small variance of searching cycles is proposed in this paper for a multi-input multi-output(MIMO) system. Small variance in number of searching cycle is achieved by applying parallel partial Euclidean distance (PED) calculation units to the one-node-per-cycle architecture. Since the proposed architecture is able to evaluate more children nodes in a single cycle, average processing cycles and error performance are significantly improved with a per-block run-time constraint. Our proposed parallel architecture increases the complexity about two times, but it can obtain a 2 dB gain in a 4x4 16QAM system when the runtime constraint is 7 cycles.

1. Introduction

A large number of work involving the physical-layer study of MIMO techniques have been done in the past decade. The optimal MIMO detector, maximum likelihood (ML) decoder, is infeasible due to high complexity when large number of antenna is used together with higher modulation constellation [1]. Efficient algorithms such as sphere decoder (SD) have been proposed to reduce the complexity of ML. Among the various variation of SD algorithms, Schnorr-Euchenr SD (SE-SD) and K-Best (KB) are applied in the implementation of [1] and [2]. KB architecture guarantees a fixed throughput and a fully pipelined architecture by restricting the number of survived node per depth [2]. However, such simplification causes severe performance degradation and increases hardware (HW) complexity. On the other hand, SE-SD is the more attractive approach as it offers lower hardware complexity and a better error rate performance compared to KB. In [1], an efficient state-of-the-art SE-SD architecture based on one-node-per-cycle strategy is presented. The Architecture of [1] reduces the circuit complexity by employing the l^{∞} norm and direct SE enumeration scheme with PSK enumeration.

A considerable problem of SE-SD is the fact that the searching complexity critically depends on the a-priori choice of the sphere radius [4]. A technique known as radius reduction with Schnorr-Euchner (SE) enumeration allows us to avoid this problem. However, the detection effort varies randomly according to the received SNR and channel matrix, so the computational throughput is non-deterministic. In practice, the maximum detection effort must be limited in SE-SD because the effort to find the solution may sometimes even corresponds to an exhaustive search. To limit the maximum detection effort is called the runtime constraint in this paper. Since run-time constraint of SE-SD is the cause of performance degradation, further improvement in reducing the average detection effort is important. In [3], we described various conventional schemes to reduce the searching cycles for practical implementation such as storage-pruning, antenna ordering, and etc. However, we did not consider the variance of searching cycle in [3]. Though the average throughput is reduced, large variance of searching cycles leads to performance degradation when run-time constraint method is applied to SE-SD. In [5], potential candidates are evaluated in terms of probability in descending order so that more promising candidates can be found earlier in the search. However, probabilistic search, which requires prohibitively large memory size, is practically infeasible.

In this paper, we propose a detector algorithm which finds the ML solution earlier by applying parallel partial Euclidean distance (PED) calculation units to the one-node-per-cycle architecture, thus stabilizing the instantaneous throughput. The proposed architecture has almost no performance degradation with runtime-constraint. An efficient minimum (MIN) search scheme is also proposed for parallel processing.

The rest of this paper is organized as follows. In Section 2, the algorithm of SE-SD is presented. The proposed architecture is described in Section 3, and we conclude the paper in section 4.

2. Schnorr-Euchner Sphere Decoding

We consider a spatial multiplexing MIMO system with N_t transmit and N_r receive antennas. The transmitter sends N_t spatial streams. Assume that the transmitted symbol is taken from a Gray-labeled M-QAM (or M-PSK) constellation ($M = 2^q$). At once, the transmitter maps one $qN_t \times 1$ coded bit vector $\mathbf{x}$ onto a $N_t \times 1$ symbol vector $\mathbf{s}$. The transmission of vector $\mathbf{s}$ over MIMO channels can be modeled as $\mathbf{y} = \mathbf{Hs} + \mathbf{n}$, where $\mathbf{y}$ is an $N_r \times 1$ receive signal vector. $\mathbf{H}$ is an $N_r \times N_t$ MIMO channel matrix which is i.i.d. zero-mean unit variance complex Gaussian matrix, perfectly known to the receiver. $\mathbf{n}$ is a vector of independent zero-mean complex Gaussian noise entries with variance $N_0 / 2$.

Depth-first SD algorithm can be divided into two parts, the first part is the partial Euclidean distance (PED) calculation and the second part is the tree traversal. The following inequality expresses the sphere constraint [1]:

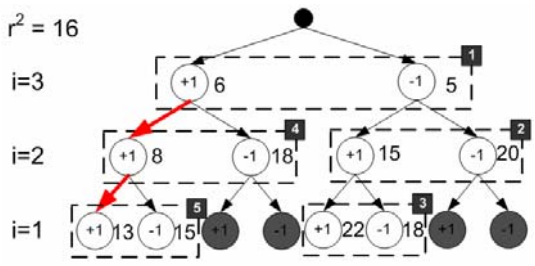

Figure 1. Example of SE-SD (3x3, BPSK)

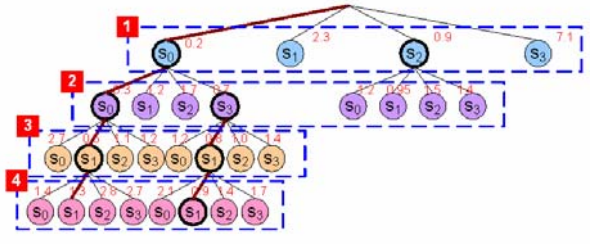

Figure 2. Example of modified tree-searching strategy (L=2)

$$\left\|\mathbf{y}-\mathbf{Hs}\right\|^2 < r^2 \ . \qquad (1)$$

The left part of inequality (1) can be decomposed into PEDs as

$$\left\|\mathbf{y}-\mathbf{Hs}\right\|^2 = \left\|\hat{\mathbf{y}}-\mathbf{Rs}\right\|^2 = \sum_{i=1}^{N_t}\left|\hat{y}_i - \sum_{j=i}^{N_t} r_{ij}s_j\right|^2 = \sum_{i=1}^{N_t} T_i\left(\mathbf{s}^i\right) \qquad (2)$$

where $\hat{\mathbf{y}} = \mathbf{Q}^H\mathbf{y}$, $\mathbf{Q}$ and $\mathbf{R}$ are the QR decomposition of $\mathbf{H}$, and r_{ij} is the element of upper triangular matrix $\mathbf{R}$. $\hat{y}_i$ and s_j are the elements of $\hat{\mathbf{y}}$ and $\mathbf{s}$, respectively. $T_i\left(\mathbf{s}^i\right)$ is called PED. PED can be re-written for efficient implementation as

$$T_i\left(\mathbf{s}^i\right) = \left|b_{i+1} - r_{ii}s_j\right|^2 + T_{i+1}\left(\mathbf{s}^{i+1}\right), \qquad (3)$$

where $b_{i+1} = \hat{y}_i - \sum_{j=i+1}^{N_t} r_{ij}s_j$.

An efficient SD uses the one-node-per-cycle architecture which calculates PEDs of all children nodes of a mother node [1]. Fig. 1 shows a simple example of tree searching and tree traversal of depth-first SD when $N_t = 3$ and $M = 2$. The number beside each circle (node) is the accumulated PED of the node. In this paper, tree level i is presented in descending order. A dotted rectangle represents the nodes which are calculated at the same time. Dark gray nodes are pruned nodes because the accumulated PEDs of their mother nodes already exceed the radius r.

In [1], the norm calculation in (3) is approximated to the l^∞ - and l^2 - norm to reduce the complexity.

In [3], some techniques such as radius update with SE enumeration, storage pruning, and antenna ordering which enhance the efficiency of depth-first SD are presented. The strict SE enumeration selects the preferred child with the smallest PED for forward and backward recursion of the tree-searching algorithm. An exhaustive search becomes the bottle-neck of the critical path in the one-node-per-cycle SE-SD architecture. Authors in [1] solved this problem through sorted lists generation. After calculating b_{i+1} in (3), signal constellation points can be grouped into 3 PSK-subset according to their distance from the origin. Then, ordering can be performed according to the position of b_{i+1}. If the region to which b_{i+1} belongs is known, the ordering of each subset is given a priori before calculating PED. PED calculation is only performed for the preferred children in each subset which has the minimum PED. Then, the minimum PED among 3 preferred children from subsets is searched using 2 comparators in 2 comparator steps. This scheme reduces area complexity by ignoring the remaining children of each subset.

3. Proposed Architecture

3. 1 Effect of Parallelism of PED Calculation

SE-SD has the fastest average processing cycle when implemented with the various options in [3]. However, the number of visited nodes varies according to channel gain and thermal noise. Moreover, the characteristic of R matrix is that the expectation values of the diagonal terms decreases as row index is increases, which makes r_{N_t,N_t} value is the smallest among the diagonal entries. Small diagonal term increases the probability of wrong selection at higher level of the tree [5]. Therefore, tree-searching requires large amount of processing cycles for backward recursion. For example, if the symbol '+1' is selected at i = 3 in figure 1, ML-solution can be found within 3 cycles.

To evaluate the more promising candidate at an earlier stage, we propose a more parallel metric calculation unit (MCU) to calculate PED. To adopt parallel MCUs to SE-SD, some modification of SE algorithm is required. Originally, SE-SD evaluates children of one mother node, then, picks the node, which has the smallest PED as the next mother node. If SE-SD meets a leaf or dead node, backward recursion which evaluate first untried node in the storage is performed in depth-first manner. However, the proposed parallel architecture evaluates L mother nodes at once where L is equivalent to the number of parallel MCUs. After evaluating children of L mother nodes, SE-SD finds L nodes which have the minimum PED among $L \times M$ children. The nodes which are not selected are visited later. In the case of backward recursion, it also chooses L mother nodes as the next mother nodes, but the depth of each mother node may not be same. Figure 2 shows a simple example of modified tree-searching strategy in a 4x4 QPSK configuration. In this example, original SE-SD spends 7 cycles to find the ML solution, but modified

SE-SD finds the ML solution in 4 cycles. The modified tree searching strategy has an additional benefit. If the ML solution comes from one of the descendants of s2 in level one, modified SE-SD saves more cycles during backward recursion compared to the original SE-SD because modified SE-SD already performed the calculation for children of s2 in level two.

Figure 3 and 4 show the CDF curves of searching cycles and the BER performance obtained through computer simulation which applies the same condition used for figure 2. When the number of parallel processing units increases, the ML solution can be found earlier, and the performance with run-time constraint is also increased. It implies that evaluating more nodes at a time improves the probability of finding the ML solution earlier. D_ave(7) in figure4 represents the runtime constraint, which means that SE-SD stops after 7 cycles. At $L=2$, SE-SD already achieves almost ML performance with no severe performance degradation. Thus, we choose the L as 2 for the proposed architecture.

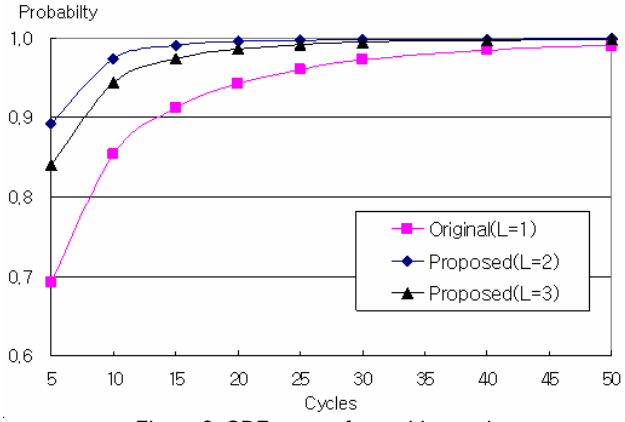

Figure 3. CDF curve of searching cycles

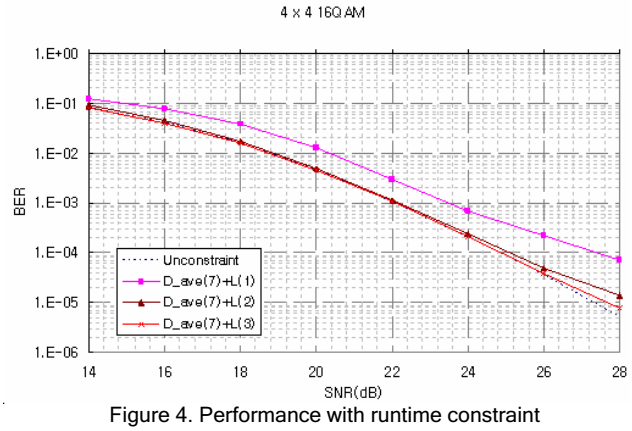

Figure 4. Performance with runtime constraint

3. 2 Hardware Architecture

It is possible to implement the proposed SE-SD architecture by modifying the state-of-the-art SE-SD architecture [1] as illustrated in figure 5. The bottle neck of this proposed architecture lies at the searching for 2 MIN selection due to SE enumeration. To find 2 MIN children among $2M$ children, $2(2M-1)+1$ comparators are required with bubble sorting ($q+2$ comparator steps). To

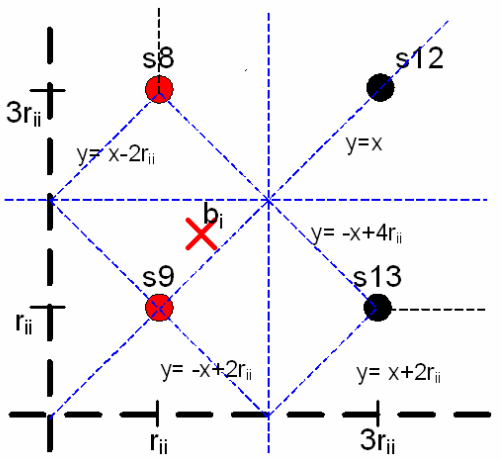

Figure 6. Decision regions to select 2 MIN-PED nodes

TABLE I. COMPLEXITY COMPARISON

	[2]		Proposed	
Antenna	4x4			
Modulation	16 QAM	64QAM	16 QAM	64QAM
# of adders	48	108	104	254
# of registers (bit)	1287	3413	2574	6826

alleviate the complexity, 2 MIN nodes of each MCU are selected directly by using decision region of QAM signal constellation in the forward recursion. At first, 2 MIN nodes among M children are selected at each MCU. Then, 2 MIN nodes are selected among four nodes. Directly choosing 2 MIN values at each MCU can be done with signal constellation. After the calculation of b_{i+1}, the decision region of b_{i+1} can be found, we then choose the first MIN node and second MIN node. For second MIN node, the decision regions are illustrated in figure 6. 8 comparators are required to know the region of b_{i+1}. For backward recursion, this proposed architecture incurs slight complexity increment. Six sorted lists from two MCUs are generated for backward recursion, while architecture [1] generates three sorted list. Thus, 2 MIN nodes selection among 2 smallest nodes in all sorted lists is required for backward recursion.

Table 1 shows the estimated hardware complexity. In this analysis, the symbols are represented by integer to reduce the number of multipliers, and a 12 bit fixed point calculation is assumed. Adder equivalent units such as a subtractor and a summation are included into the number of adders. As compared to the conventional architecture, the proposed architecture requires about two times of hardware complexity. However, proposed architecture finds more reliable candidates earlier compared to conventional SE-SD architectures.

4. Conclusion

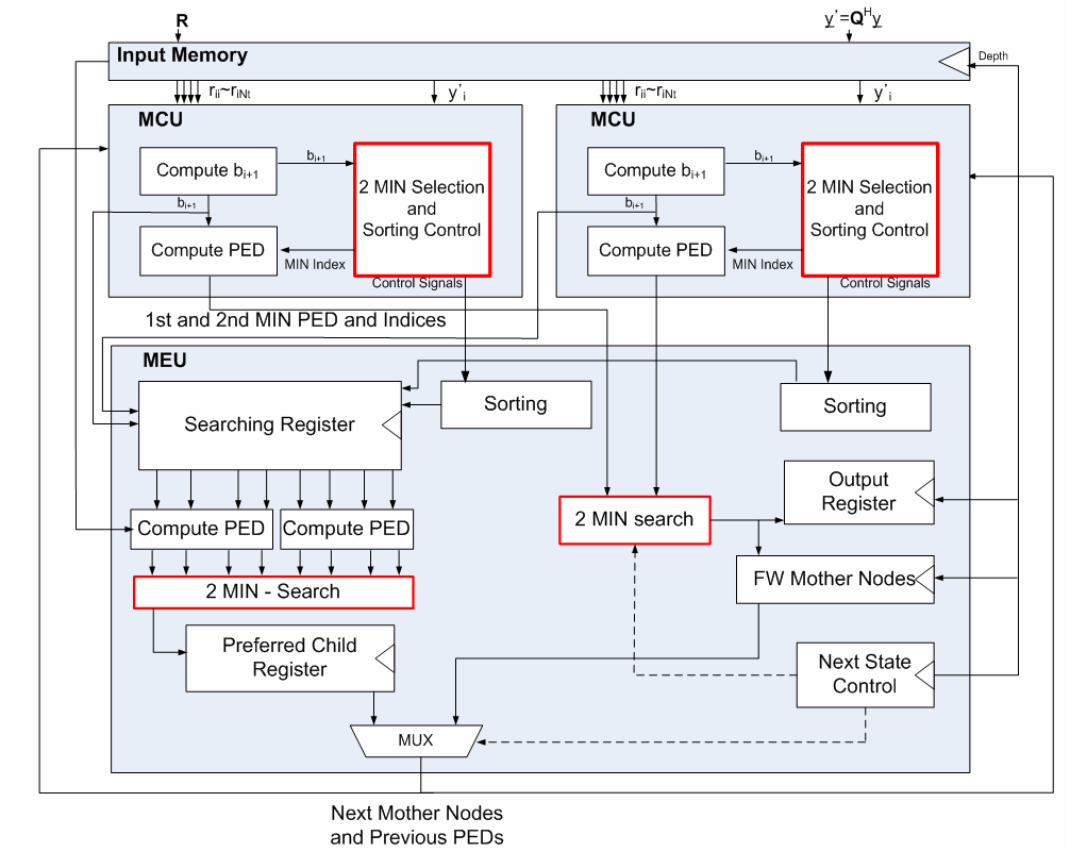

Figure 5. Block diagram of proposed architecture

Since, the processing cycles of Schnorr-Euchner Sphere Decoder varies randomly varied with MIMO channel matrix and AWGN noise, operating cycle of Sphere Decoder should be restricted for real implementation. However, constrained Sphere Decoder causes severe degradation in error performance. In this paper, we proposed the SE-SD architecture for run-time constraint by adapting the parallel tree searching with SE enumeration. The proposed architecture achieves performance gain due to faster searching compared to conventional architecture when runtime constraint is applied. To adopt the parallel processing, efficient MIN-selection using QAM signal constellation is also introduced during the forward and backward recursion. Although the complexity of the proposed architecture increases about two times, it can obtain a significant 2 dB gain in a 4x4 16QAM system when the runtime constraint is 7 cycles.

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