# Implementation of Low Power Consumption of Neuromorphic Device s

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## Abstract:

For a large scale artificial neural network, it is desirable that a neuromorphic device constructing presents low power consumption.

Previously, we proposed a cell body model with a reduced mounting area, with a power consumption was 4.2 [mW]. In this model, the gate voltage of the N-channel type MOSFET (NMOS) as a negative resistance device was more than the voltage that the IC can withstand.

In this paper, we reduce the gate voltage of this NMOS, resulting in a neuromorphic device with a gate voltage lower than 2.2 [V]. Furthermore, it is clearly shown that its power consumption is approximately 16.6% lower than the previous proposed model.

## 1. Introduction

Brain neural network presents excellent information processing mechanism, leading many investigators to model biological neurons and their networks Recent neural networks studies have been undertaken with the purpose of applying engineering to the brain function [ref. 1, 2, 3, 4]. As a method for modeling the information processing function of the brain, the artificial neural network (ANN) has been suggested. Therefore, it is necessary to construct ANN using neuromorphic devices, which is the features of the neuron. When a large-scale ANN is constructed, it is desired that its neuromorphic device has a small area and low power consumption.

Analog LSI neuron model for similar biological excitable membrace operation has been proposed by Kano et al [ref. 5]. The model simulates excitations observed in neurons of the living body using voltage-controlled negative resistance characteristics. The action potential generation mechanism is similar to the neurons of the living body. As a result, this model presents vertical length of 60 [μm]; horizontal length of 180 [μm]; and power consumption of approximately 240 [μW] without input and 8.3 [mW] at firing time.

Previously, we proposed a cell body model [ref. 6] with a reduced the area, using the parasitic capacitance and the N-channel MOSFETs (NMOS). The power consumption of this model is approximately 4.2 [mW]. However, the gate voltage of the NMOS, which is a negative resistance device, became greater than the breakdown voltage. In this paper, we study the implementation of a neuromorphic device with low power consumption by focusing on the gate voltage of NMOS as a negative resistance device.

## 2. Neuromorphic device

Figure 1 shows a circuit diagram of the proposed neuromorphic device. Circuit parameters are $M_N = 60$, $M_D = 0.6$, $M_C = 1$, $M_R = 0.67$, $M_T = 20$, and power-supply voltage $V_A = V_D = 1.8$[V]. Furthermore, $C_{g1}$, $C_{g2}$ and $C_M$ are parasitic capacitances.

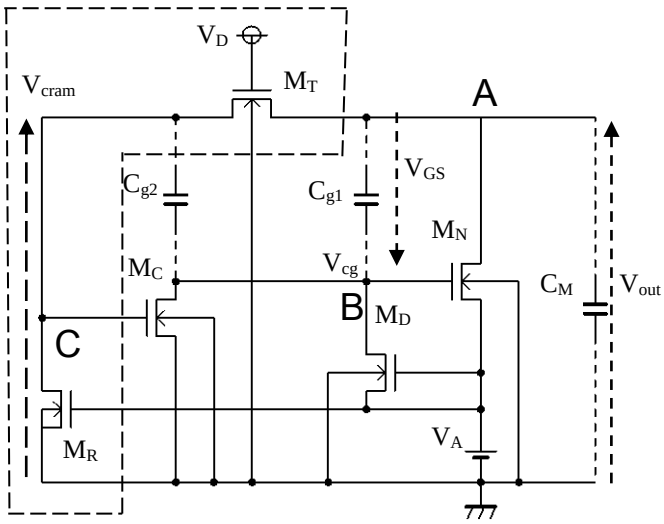


Figure 1 Proposed neuromorphic device

The principle of Figure 1 is shown as follows. In the initial condition, if $V_{out}$, $V_{cg}$ and $V_{cram}$ is 0 [V], drain-source voltage of $M_T$ and $M_R$ are both 0 [V]. Hence, there is no drain-source current on $M_N$ and $M_C$. the gate-source voltage of $M_C$ and $M_N$ is also 0 [V], resulting in a null drain-source current on $M_C$ and $M_T$. $C_{g1}$ and $C_{g2}$ are supplied with the charge of $V_A$ through $M_D$. Since $C_{g1}$ charge does not flow through $M_T$, it flows into $C_M$, resulting in small $V_{out}$. Furthermore, when there is electric potential difference of drain-source voltage of $M_T$ and $M_R$, current flows from the former's drain to the latter's source. When $V_A$ increases, $C_{g1}$ and $C_{g2}$ are charged, and there is an increase on $M_N$ gate-source voltage ($V_{GS}$). $V_{GS}$ is greater than threshold voltage, results in large drain-source current of $M_N$. Because W/L of $M_N$ is greater than W/L of $M_T$ and $M_R$, the surplus current does not flow in $M_T$ nor $M_R$. As a result, it flows into $C_M$, and $V_{out}$ rises up. In addition, $V_{cram}$ also rises up and gate-source voltage of $M_C$ becomes more the threshold voltage. Therefore, drain-source current of $M_C$ begins to flow. $M_C$ pulls out the charge of $C_{g1}$ and $C_{g2}$, and then $V_{GS}$ goes down. As a result, when $V_{GS}$ is ncar to 0 [V], current does not flow in $M_N$. When the charge accumulated in $C_M$ dissipates through $M_T$ and $M_R$, $V_{out}$ goes down, and then $V_{cram}$ also goes down. Hence, the current does not flow

in $M_C$. The proposed neuromorphic device repeats the oscillation by again accumulating the charges in $C_{g1}$ and $C_{g2}$ through $M_D$ from $V_A$.

Figure 2 shows the output waveform while Figure 1 shows the gate potential of $M_N$. It can be seen that the gate potential of the NMOS as a negative resistance device is suppressed to less than or equal to the breakdown voltage, 2.2 [V].

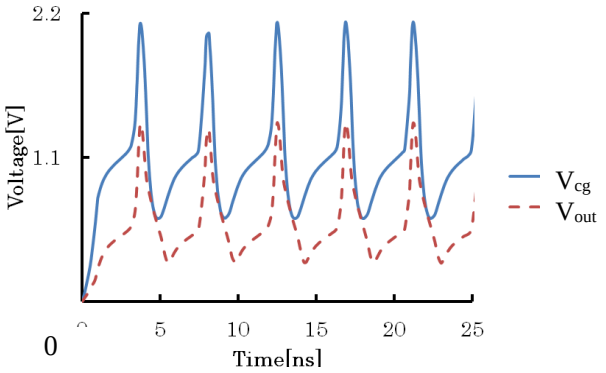


Figure 2 Voltage characteristics of proposed neuromorphic device

On the conventional model, $V_{cg}$ is the gate voltage of NMOS as a negative resistance device. It can be expressd as

$$V_{cg} = V_{out} + V_{GS} \qquad (1)$$

In this equation, $V_{out}$ is voltage across $C_{M.}$. $V_{GS}$ is the gate-source terminal voltage of $M_N$. From the above equation, $V_{cg}$ is reduced by reducing $V_{out}$ or $V_{GS}$. In order to reduce the $V_{cg}$, the following improvements are required to the conventional model.

(i) Insertion of $M_T$
(ii) Connection of the parasitic capacitance between $V_{cg}$ and drain-source terminal of $M_T$
(iii) Increase of the aspect ratio of $M_N$

Figure 3 shows a circuit diagram of a clamp circuit including a $M_T$. In this figure, circuit parameters are $M_T$ = 20, $M_R$ = 0.67, $V_A$ = $V_D$ = 1.8 [V]. In Figure 1, the part surrounded by a dotted line corresponds to Figure 3. Figure 4 shows the characteristics of the latter. When the peak-to-peak voltage of $V_{out}$ = ±1.8 [V] and frequency is 333 [MHz], it shows $V_{out}$ and $V_{cram}$ characteristics. It can be seen that $V_{cram}$ is clamped by approximately ±1 [V]. Thus, by inserting $M_T$, point C in Figure 1 has a potential lower than $V_{out}$..

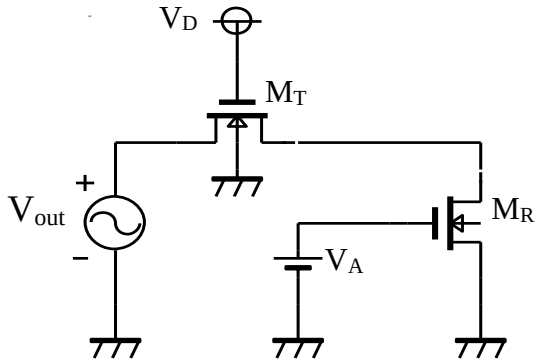


図 3 Clamp circuit

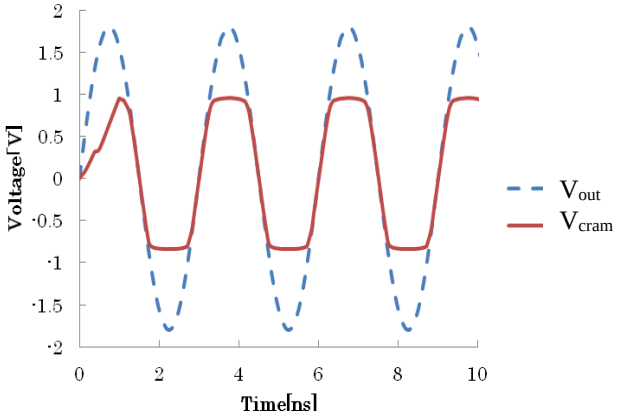


図 4 Voltage characteristics of clamp circuit

In the conventional model, the gate of $M_C$ was connected to $V_{out}$. Therefore, the parasitic capacitance was connected only between $V_{out}$ and $V_{cg}$. Hence, $V_{cg}$ was influenced by only $V_{out}$ and $V_{GS}$ according to the parasitic capacitance between A and B. However, in the proposed neuromorphic device, the gate of $M_C$ is connected to C by inserting the $M_T$. Further, in the conventional model, the parasitic capacitance between A and B was composed by the parasitic capacitance between drain and gate of $M_C$ and between gate and source of $M_N$.Therfore, by connecting the gate of the $M_C$ in C, appears a parasitic capacitance between B and C. The potential of $V_{cg}$, which was only influenced by $V_{out}$ in the conventional model, is reduced by the influence of $V_{cram}$.

Then, the aspect ratio of the $M_N$ was increased. Consequently, when $V_{out}$ rises, the drain-source current of $M_N$ increases. Since the amount of current flowing into the $C_M$ increases, $V_{out}$ increases. When $V_{out}$ rises fater than a conventional model, $V_{cram}$ rises fast, too. Therefore, the drain-source current of $M_C$ flows faster than the conventional model. It is possible to reduce $V_{cg}$ by withdrawing charges from $C_{g1}$ and $C_{g2}$ before the potential of $V_{cg}$ reses high. Figure 5 shows changes in $V_{cg}$ of the proposed neuromorphic device when changing the aspect of $M_N$. It is seem that, by increaseing the aspect ratio of the $M_N$, $V_{cg}$ reduces.

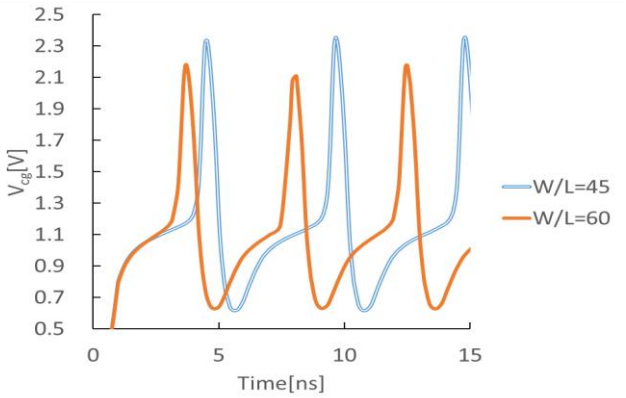


Figure 5 $V_{cg}$ characteristics regarding the aspect retio in $M_N$

## 3. Refractory period

Figure 6 shows the refractory period characteristics of the proposed neuromorphic device. Δt represents a time interval to input $I_{in}$ as reproduction signal of another neuron model from outside. $V_{out\,1}$ and $V_{out\,2}$ shows the peak value of $V_{out}$ after the first and second time of $I_{in}$, respectively. Hence, neuromorphic devices are the separately excited cell body model. Figure 6 represents the change in the firing condition for the input period. It is shown that the neuromorphic device does not fire on the second time of $I_{in}$ when the input period Δt is short. Therefore, it can be seen that neuromorphic device has a refractory period characteristics.

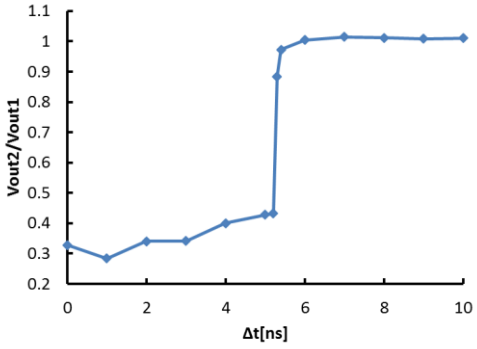


Figure 6 Refractory period characteristics

Figure 7 shows the relative refractory period characteristics of the proposed neuromorphic device. The figure represents the change in the firing state for second input of neuromorphic device, when Δt is 4 [ns] and the peak value of input has been increased. In this figure, it is shown that the neuromorphic device can oscillate when $I_{in}$ increase, while the refractory period. Therefore, it can be seen that the proposed neuromorphic device has a relative refractory period characteristics.

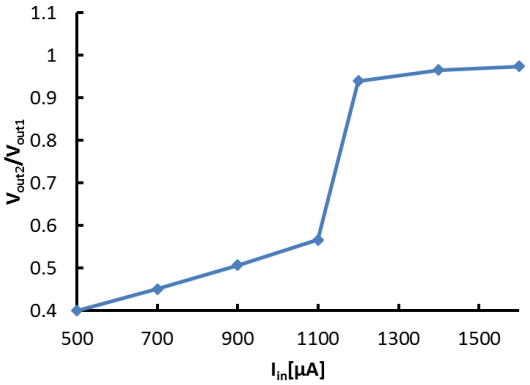


Figure 7 Relative refractory period characteristics

## 4. Chaotic response

Figure 8 shows the input-output frequency characteristics of the proposed neuromorphic device. $f_{in}$ represents the frequency of $I_{in}$, while $f_{out}$ indicates the oscillation frequency of $V_{out}$. Drawing effect 1:1, 1:2 and 1:3 can be observed. Figure 9 shows the attractor of the proposed neuromorphic device when input period is 2.75 [ns] ($f_{in}$ = 0.36 [GHz]). From the above reason, it suggests that chaotic response is obtained from the proposed neuromorphic device.

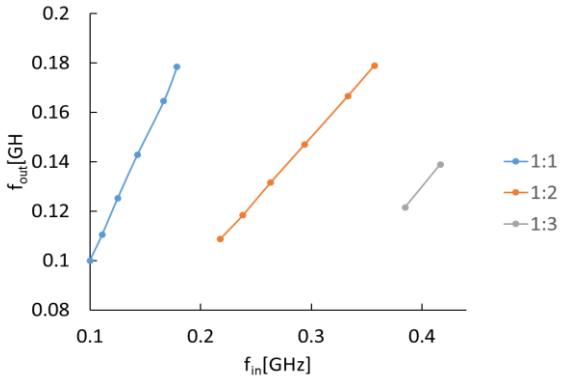


Figure 8 Input-output frequency characteristic

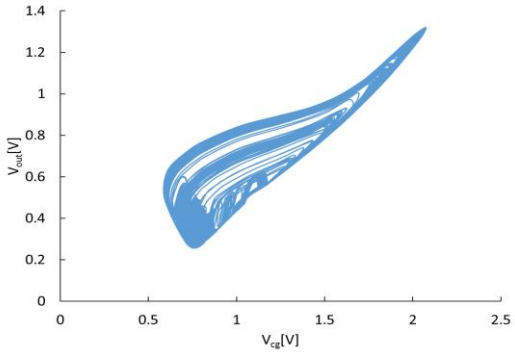


Figure 9 Attractor

## 5. Layout

Figure 10 shows layout diagram of the neuromorphic device. From Figure 3, the vertical length is approximately 9.6 [μm], the horizontal length is approximately 14.9 [μm]. Therefore, the proposed device mounting area is

approximately 142.6 [μm$^2$], which is almost same as that of the conventional model.

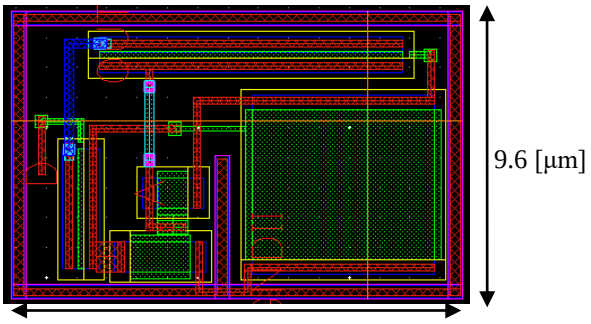


Figure 10 Layout of the proposed neuromorphic device

## 6. Power consumption

Figure 11 shows the current characteristics of $I_A$ and $I_D$, which is flowing through $V_A$ and $V_D$, respectively. The power consumption of the proposed neuromorphic device is approximately 696.8 [μW]. On the other hand, the power consumption of a conventional device is about 4.2 [mW]. Table 1 compares power consumption of both devices. It shows reduction of up to 16.6% when compared with the latter.

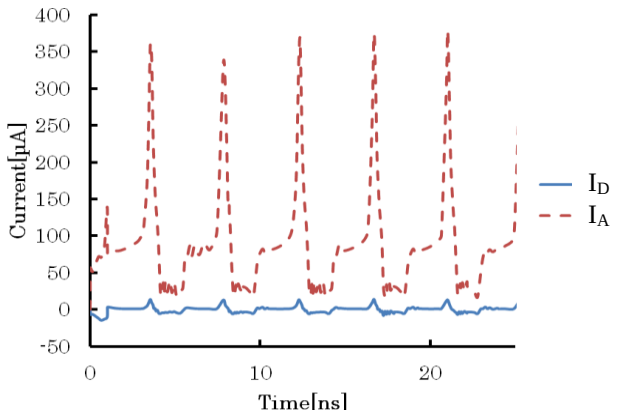


Figure 11 Current characteristics of power supply

Table 1 Power consumption comparison

| | Power consumption |
|---|---|
| Conventional model | 4.2 [mW] |
| Proposed neuromorphic device | 696.8 [μW] |

## 7. Conclusion

In this paper, we examined the implementation of low power consumption of a neuromorphic device by focusing on the gate voltage of NMOS as a negative resistance device. As a result, we constructed a neuromorphic device with a gate voltage of less than 2.2 [V]. Furthermore, it was clearly shown that its power consumption was reduced to approximately 16.6%, when compared with the conventional model.

In future work, we will construct a large-scale neural network using a neuromorphic device.


## Acknowledgements

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