# A 1V/1.8V Ultra Low Noise LDO for 5.6GHz PLL Applications

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**Abstract:** This paper presents a low noise low drop voltage (LDO) for 5.6GHz PLL application. The proposed LDO employs internal RC-Filter with multi-layer capacitor at the output of the bandgap reference (BGR) to achieve ultra-low noise at interest frequencies. It is also a mode changeable LDO so that the output voltage level can be 1V/1.8V. The 4-bits controlled resistor ladder is adopted to compensate the process voltage temperature (PVT) variation. The highest output noise of the LDO are 5.68fV$^2$/Hz and 23fV$^2$/Hz at 10 kHz in 1V/1.8V mode respectively. The proposed LDO is implemented in CMOS 65nm technology with the die size is 460µm x 290µm.

*Keywords*—**Ultra Low Noise , LDO, 6.5GHz PLL**

## 1. Introduction

The recent trend on electronic design is lowering the fabrication process, size of transistor and operation voltage is decreased. By lowering the transistor size and supply voltage, the sensitivity of devices to noise becomes dominant. The second trend is the phenomenal growth in portable where devices operate using battery power source. The power provided by battery is limited and unstable, that require the power supply regulator operate with high precision and stability.

The average operating frequency of circuits are keeping increasing, that requires the synchronous circuits such as PLL and VCO should be able to operate at high frequency. For the VCO and PLL operation, the most important object that keeps circuit generating stable clock is the power supply. A low precision and stability power supply can fail all the system follows the VCO and PLL. To maintain those aspects of power supply, the precise and stable low-dropout regulator is required in the power supply line. The proposed LDO is designed with very high stability, ultra-low noise and wide bandwidth with a small size comparing to related design [1][2][3].

## 2. Proposed Low noise LDO

A conventional LDO consists of four main components: voltage reference, pass transistor, error amplifier, and resistive divider. In LDO circuit, there are many noise sources. Among these noise sources, the noise from BGR is the dominant and contributes 80% of total noise. Therefore, we focused on reducing the noise of the BGR and also enhance the noise performance of other internal nodes at the same time.

The noise from resistive divider is also take in account and can be estimated as equation (1) in 1V mode and equation (2) in 1.8V mode

$$S_{N,div} = E_{n\_R1R2R3} * \sqrt{\frac{R_1}{R_3}} \quad (1)$$

$$S_{N,div} = E_{n\_R1R2R3} * \sqrt{\frac{R_1 + R_2}{R_3}} \quad (2)$$

where En_R1R2R3 is the total noise of the divider resistors connected in series [4].

Figure 1 shows the architecture of the proposed LDO in this work. As mentioned above, the BGR noise is the dominant contribution to the total output noise of the LDO. Besides using the RC-filter to cancel the output noise of the BGR, the error amplifier of the BGR and LDO also the low noise amplifier structure presented in [5]. To reduce the area, there are three kinds of capacitors are used in parallel in schematic and overlap in layout that's called multi-layer capacitor as shown in Figure 2. In 65nm CMOS technology, the metal-insulator-metal (MIM) capacitor uses metal 7 layer, the transistor (MOS) capacitor use poly and metal 1 layers, the metal-oxide-metal (MOM) capacitor uses metal 3-to-6 layers. Thus, these MIM/MOS/MOM capacitor can be located at the same area in layout and provide a significant capacitance value for RC-filter then no external capacitor is required.

The switch MODE is used to short and open the resistor R2 to change the LDO output voltage between 1V and 1.8V mode. The output voltage of LDO is calculated as follows:

$$V_{out} = \left(1 + \frac{R_1}{R_3}\right) V_{REF} \quad \text{or} \quad V_{out} = \left(1 + \frac{R_1 + R_2}{R_3}\right) V_{REF} \quad (3)$$

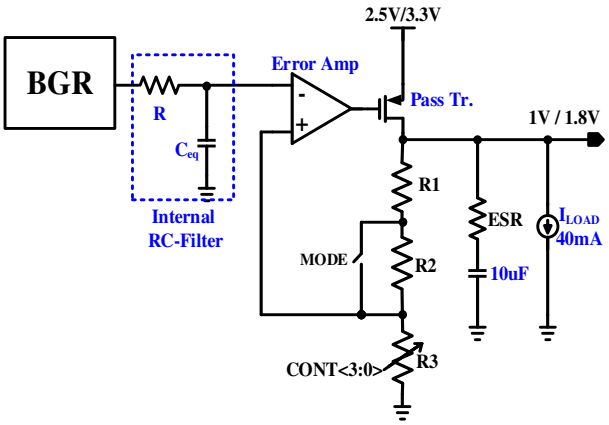


**Figure 1 Proposed Ultra Low Noise LDO**

Controlled by 4 trimming bits, the R3 is a changeable resistor and has 16 values. The outputs are designed to be 1V/1.8V at the center value of control bits when the MODE switch is ON and OFF respectively.

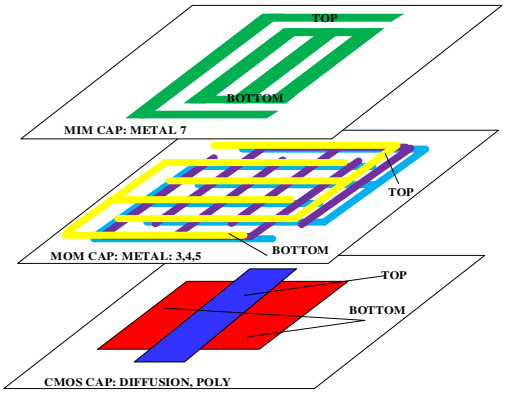


**Figure 2 Multi-layer capacitor structure**

## 4. Simulation Results

The proposed LDO is implemented in CMOS 65nm technology and simulated using Cadence Spectre. The active area of the LDO is 460µm x 290µm and the top layout is shown in Figure 3. The LDO has 1V and 1.8V output voltage with the input voltage is 2.5V.

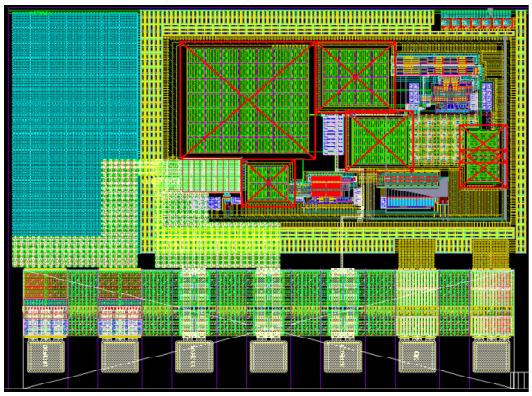

**Figure 3 Proposed Ultra Low Noise LDO Layout**

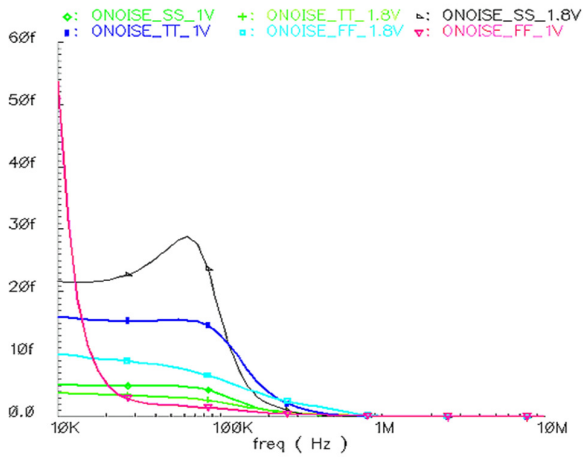


**Figure 4 Proposed LDO Output Noise Simulation Results**

The output noise of the LDO is illustrated in Figure 4. In 1V mode, the highest noise only 53.7fV2/Hz at 10 kHz in SS corner and in 1.8V mode is 28.8fV2/Hz at 65 kHz in SS corner. The post simulation in different corners of the output noise at interested frequencies are shown in Table 1 at 20mA load current.

**Table 1. Output Noise ($V^2$/Hz) performance summary**

| MODE | Freq. | SS/2.25V/90° | TT/2.5V/50° | FF/2.75V/-30° |
|---|---|---|---|---|
| 1V MODE | 10KHz | 5.37E-14 | 3.91E-15 | 2.28E-15 |
| | 100KHz | 2.09E-16 | 5.05E-16 | 7.19E-16 |
| | 10MHz | 1.05E-21 | 9.82E-22 | 9.73E-22 |
| 1.8V MODE | 10KHz | 2.37E-14 | 1.66E-14 | 1.04E-14 |
| | 100KHz | 7.75E-16 | 2.06E-15 | 3.47E-15 |
| | 1MHz | 3.36E-19 | 8.84E-19 | 3.85E-18 |

## 5. Conclusions

The ultra-low noise LDO is proposed and implemented in this paper. The low noise amplifier is applied in both BGR and LDO design for optimizing noise of the overall LDO. The RC filter is applied at the output of the BGR for reducing the noise generated by BGR, thus contributing to reduce the total noise of the LDO. The multi-layer capacitor is applied on the RC filter to reduce the total design size. The LDO is designed to operate in two mode that generate output at 1V and 1.8V. The worst output noise performance of the LDO are 53.7fV2/Hz at 10 kHz and 28.8fV2/Hz at 65 kHz in 1V/1.8V mode. The die size is 460µm x 290µm. While obtaining a very high noise performance with a small size, others regulation performance such as line regulation, load regulation, temperature regulation, and PSRR are well maintained.

With the impress noise performance, the proposed LDO is applied to power up the 5.6GHz PLL design, which requires an extremely accuracy and stable voltage supply. With the small size, out proposed LDO can be integrated to other RF application which requires ultra-low noise and high stability power supply network.

**Table 2. Performance Comparison**

| | [1] | [2] | [3] | [This work] |
|---|---|---|---|---|
| **Process** | 0.18µm | 0.18µm | 0.25µm | 65nm |
| **$V_{IN}$** | 3V | 1.8V | 2-2.5V | 2.5V |
| **Max Load** | 100mA | 50mA | 50mA | 100mA |
| **Noise (V/sqrtHz)** | 56.4µ (1KHz-1MHz) | 270n (100KHz) | 32n (100KHz) | <73.2n (*) (10kHz-1MHz) |
| **PSRR** | 71.6dB | 60dB | 25dB | 67dB |
| **Current Consumption** | - | 50µA | 120µA | 180µA |
| **Die Area** | - | 0.14mm$^2$ | 0.88mm$^2$ | 0.1334mm$^2$ |

(*) maximum output noise: 73.2nV/$\sqrt{Hz}$= 53.7fV$^2$/Hz as shown in Table 1.

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