A Design of High Sensitivity Bridge Circuit using only Two Differential Resistive Sensor

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Abstract: A novel resistance difference to voltage conversion (ΔRVC) circuit that uses a linear CMOS voltage to current converter (VIC) and an operational amplifier (op-amp) with a low cost and high accuracy measurement system is designed. This proposed circuit was designed for one-chip fabrication and consists of a VIC, an op-amp and a two resistive sensors. The main characteristic of this circuit configuration does need any matching for resistive element and has an advantage of twice the sensitivity compare to a conventional bridge circuit. Simulation results show that the resistance difference to voltage conversion circuits agree with theoretical equation.

Keywords-- **Analog circuits, resistive sensor, voltage-to-current converter, CMOS op-amp**

1. Introduction

The sensor technology is one of the important fields in industrial automation. It has some comprehensive applications in industry realm, agriculture and even in national defenses. In past few years, the sensing resistors were manufactures by polycrystalline silicon membrane [1]. The resistance difference circuit is important in processing the signal of sensor, *e.g.* the electronic scale in determining its sensitivity [2]. Generally, the resistance difference can be detected using bridge circuits.

Figure 1 shows the conventional bridge circuits in obtaining the resistance difference. In figure 1 (A), uses one resistor for sensing while the other resistors use to match the sensitivity and linearity error of the output when it is too large. While figure (B) and (C) are the improve version of (A) but still linearity error still exists. While figure (D) has a better performance but the drawback requires a 4 sensing resistors and a resistor matching pairwise is needed. It also requires an instrumentation amplifier in obtaining the resistance difference [3, 4].

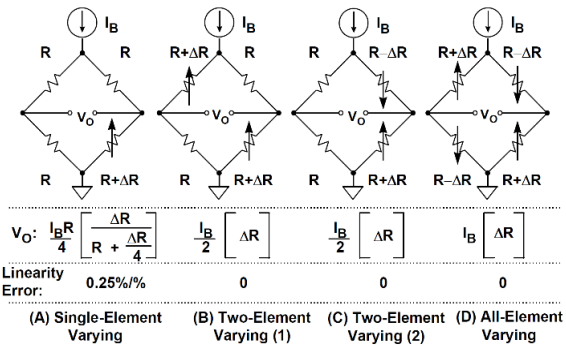

Figure 1. Conventional bridge circuit for resistance difference

This proposed resistance difference to voltage conversion (ΔRVC) circuit can solve the existing drawback from the conventional bridge circuit and uses linear voltage to current converter (VIC) and op-amp.

The rest of this paper is organized as follows. Section 2 describes operating principle and circuit configuration of the resistance difference to voltage converter. Section 3 shows the experimental and simulation results. Finally, Section 5 concludes this paper

2. Operating principle and circuit configuration of the resistance difference to voltage converter

2. 1 Operating principle

Figure 2 shows the proposed resistance difference to voltage converter. It consists of two constant current sources, two resistance sensors and an op-amp. In an ideal op-amp operation, V_{R1} is given by $V_{R1} = I_{R1} = I(R+\Delta R)$, where V_{R1} is the non-inverting voltage. And V_{R1} is the same voltage drop as V_{R2}. Then, applying KVL at output voltage node to the non-inverting and inverting input. The output voltage (V_o) can be described by the following equation:

$$V_O = V_{R1} - V_{R2} = IR_1 - IR_2 = 2I\Delta R \qquad (1)$$

As a result it can have a double sensitivity output, although it uses only two resistance sensor like in Figure 1 'B'.

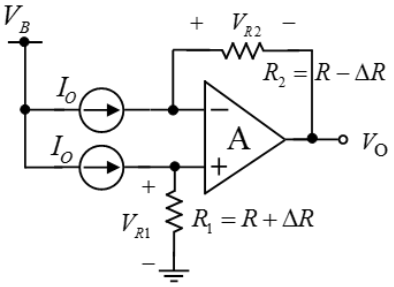

Figure 2. Operating principle of the proposed resistance difference to voltage converter.

2. 2 Review of conventional resistive-difference to voltage converter using linear LOTA

This work was supported by the IT and R&D Program of Ministry of Trade, Industry and Energy (10049192, Development of Smart Automotive ADAS SW-SoC for Self-Driving Car).

Figure 3 shows resistance difference to voltage converter using LOTA. It consists of a LOTA, an op-Amp and two resistors [5]. During the ideal operation of op-amp and VIC, i_O is defines as $i_O = g_m V_B$. Since VIC uses the configuration in figure 3, the two outputs will be the same. The output voltage can be described in equation (2).

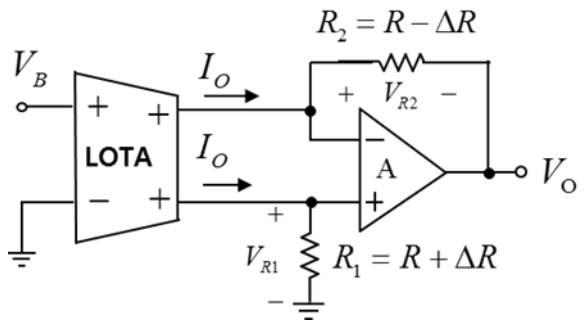

Figure 3. Block diagram of conventional resistive-difference to voltage converter using linear LOTA.

$$V_O = V_{R1} - V_{R2} = (R_1 - R_2) i_O = g_m (R_1 - R_2) V_B \quad (2)$$

If R_1, R_2 is replaced by $R_1 = R + \Delta R$, $R_2 = R - \Delta R$, therefore the obtained equation is shown in equation (3).

$$V_O = \frac{2\Delta R}{R_S} \cdot V_B \quad (3)$$

although it uses two resistance sensors as shown in figure 1 (B), the sensitivity result can be double.

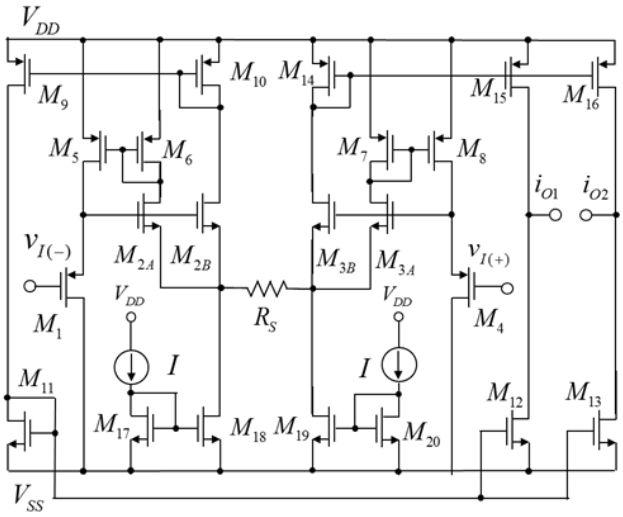

Figure 4. Circuit diagram of CMOS LOTA in conventional resistive-difference to voltage converter.

Figure 4 shows the CMOS LOTA with two current outputs. It consist of low voltage linear transconductors (M_1~M_8) and multiple current mirrors with a single current output of transconductor. In low voltage linear transconductor, when the voltages amount of $V_{GS1,4}$ changes from an increasing state to decreasing mode, the voltages in $V_{GS2,3}$ also follows with the current mirrors (M_5~M_8) for biasing, as it shown in equation (4). Therefore, the input voltage can be related to R_S and I_S, which pass on R_S.

$$V_{IN} = V_{I(+)} - V_{I(-)} = R_S (i_{D3} - i_{D2}) \quad (4)$$

Since i_{D2} is replicated by the PMOS current mirrors (M_9~M_{10}) and NMOS current mirrors (M_{11}~M_{13}) while i_{D3} is replicated by NMOS current mirrors (M_{14}~M_{16}), $i_{D2}=i_{D12}=i_{D13}$, $i_{D3}=i_{D15}=i_{D16}$. Thus, Single-output current for the final differential input voltage is given as follows:

$$i_{O1} = i_{O1} = \frac{2}{R_S} \cdot V_{IN} \quad (5)$$

Figure 5 shows linearity and control range charateristics of the LOTA of figure 4 at the load resistors R_{O1} = R_{O2} = $10k\Omega$, the degeneration resistor R_S = $10k\Omega$, and the bias current I = $100\mu A$. The linear theoretical range value is determined by $R_S I = 10k\Omega \times 100mA$. The experimental results confirmed that nearly matches with the theoretical value. However, this CMOS LOTA has the disadvantages that operates in dual supply voltage and has a complex structure.

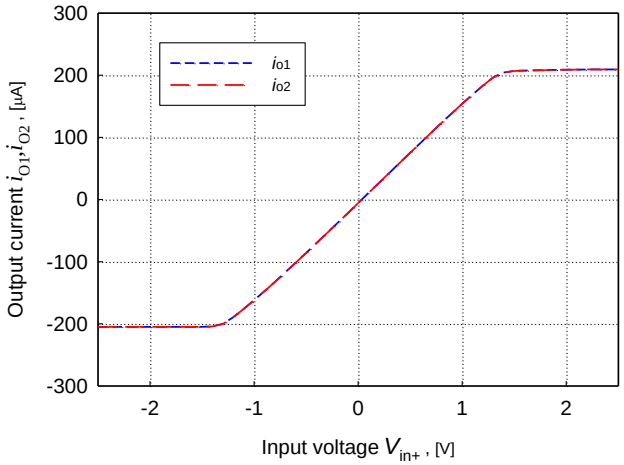

Figure 5. Characteristics of voltage-to-current for conventional CMOS LOTA.

2.3 Design of proposed resistive-difference to voltage converter using linear VIC

Figure 6 shows resistive-difference to voltage converter using VIC. It consists of a voltage-to-current converter (VIC), an op-amp and two resistors. If an ideal op-amp and VIC operation, i_O is given by $i_O = g_m V_B$. Since uses the VIC

in figure 6, which is the two has the same output. Then, applying KVL at output voltage node to the non-inverting and inverting input, the output voltage can be obatined as shown in Equations (6).

$$V_O = V_{R1} - V_{R2} = (R_1 - R_2) i_O = g_m (R_1 - R_2) V_B \qquad (6)$$

If R_1, R_2 will be replaced by $R_1 = R + \Delta R$, $R_2 = R - \Delta R$, the resulted equation is shown in (7).

$$V_O = \frac{2\Delta R}{R_S} \cdot V_B \qquad (7)$$

although it uses two resistance sensors as shown in figure 1 (B), the sensitivity result can be double.

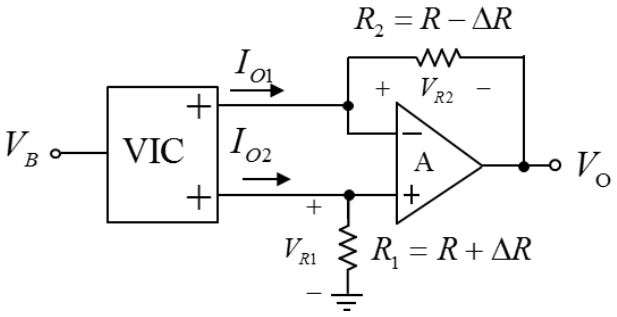

Figure 6. Circuit diagram of proposed instrumentation amplifier using proposed VIC.

2.4 Design of proposed linear voltage to current converter with two outputs

Figure 7 shows the designed VIC with two current output. It consists of current mirrors using an adaptive feedback for low input impedance (M_1, M_2), cascode current mirrors for high output impedance (M_3~M_{10}) and resistor (R) [6] due to the value of V_{sg} of M_1 and V_{gs} of M_2 fluctuates with V_C, therefore the output current can be described in equations (4) and (5).

$$-V_C - V_{gs1} + V_{gs2} + I_O R = 0 \qquad (4)$$

$$I_O = \frac{V_R}{R} \left(\because V_{gs1} = V_{gs2}, \forall V_R \cong V_C \right) \qquad (5)$$

From these the transconductance gm is given by $g_m = i_o / v_R = 1/R$. Then the replications of mirror currents of M_9 and M_{10} is caused by the cascode current mirror in I_O.

2.5 Design of CMOS op-amp

Figure 8 shows the designed CMOS op-amp, it composes of a level shift (M_{S1}, M_{S2}), a PMOS as the input stage of differential (M_7, M_8), a NMOS as the differential input (M_1 ~ M_6), a cascode amplifiers (M_9 ~ M_{14}), while the output stage of class-AB (M_{15} ~ M_{17}) and bias circuits with constant current sources.

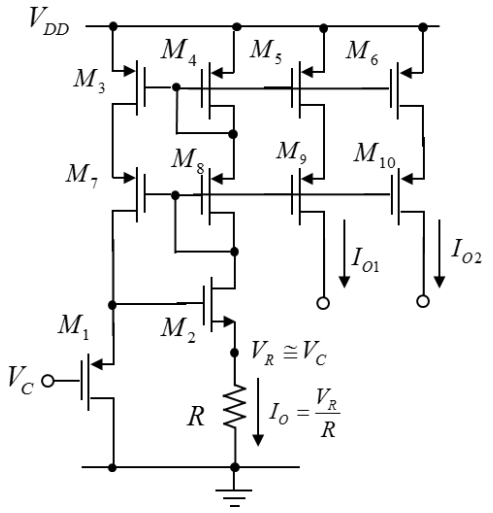

Figure 7. Circuit diagram of proposed linear VIC with two current output.

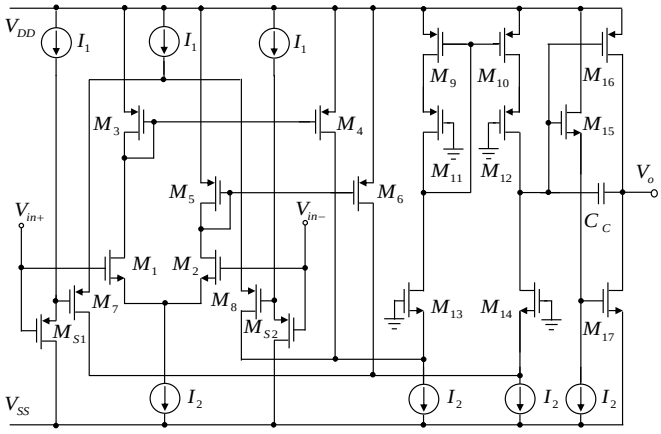

Figure 8. Circuit diagram of CMOS Op-amp.

3. Simulation results and discussion

The operating principle of proposed ΔRVC was verified by using OrCAD Pspice simulation at the full parameter of TSMC CMOS 0.35μm. The value of the device are set by V_{DD} of VIC is *5.0V*, the supply voltage range of op-amp is *±2.5V*, $R_1 = R_2 = 10k\Omega$, $\Delta R = 0 \sim 5k\Omega$, $V_C = 0.75V$, the bias currents $I = I_1 = I_2 = 20\mu A$ (op-amp) and $I_O = I_{O1} = I_{O2} = 100uA$ (VIC).

Figure 9 shows linearity and control range charateristics of the VIC in Figure 7 at the resistor $R = 10k\Omega$. Since V_R has an offset current, the theory of I_O should replace to $I_O = V_C + I_O R / R$ when $V_C = 0V$, value of I_O is around $0.25\mu A$. Therefore, when $V_C = 0.75V$, $V_R = 1V$ so it can confirm the output current I_O is $100\mu A$. Also, g_m is theoretically the same. Op-amp was simulated at load capacitance $C_L = 5pF$ as shown in figure 8. Table 1 shows the performance of the proposed op-amp.

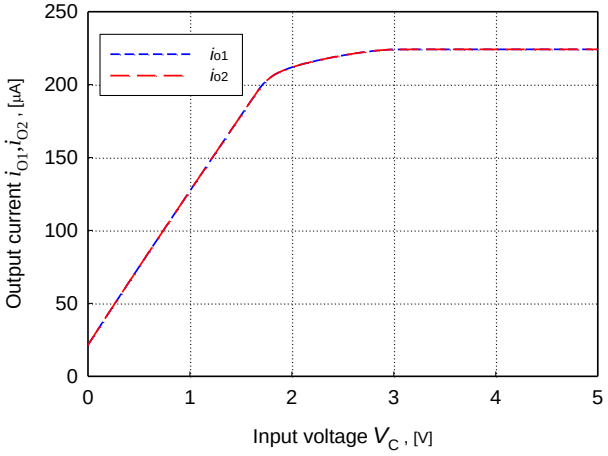

Figure 9. Caracteristics of Voltage-to-Current for proposed VIC.

Table 1. Performance o fhe proposed CMOS op-amp.

Specification	Unit	Value
Supply voltage	V	±2.5
Bias current	μA	20
Gain(dB)	dB	122
-3dB frequency	Hz	1.99
Unit gain frequency	MHz	1.18
Phase margin	Deg	62
Slew rate	V/μs	2.9
Power dissipation	mW	0.7

Figure 10 shows the characteristic of the proposed resistance-difference to voltage converter when ΔR ranges from *0* to *5k*Ω while in figure 11 shows the characteristic of the proposed resistance difference to voltage converter when ΔR is ranging from *0* to *0.5k*Ω. Therefore, theoretically, V_O is the same.

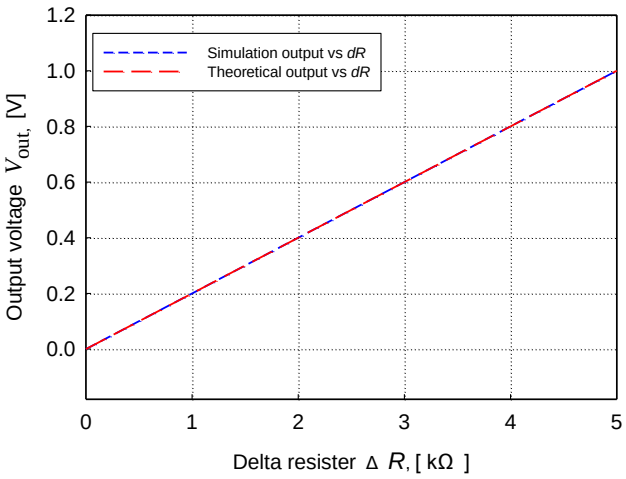

Figure 10. Characteristics of proposed resistance-difference to voltage converter when ΔR is 0 to 5kΩ.

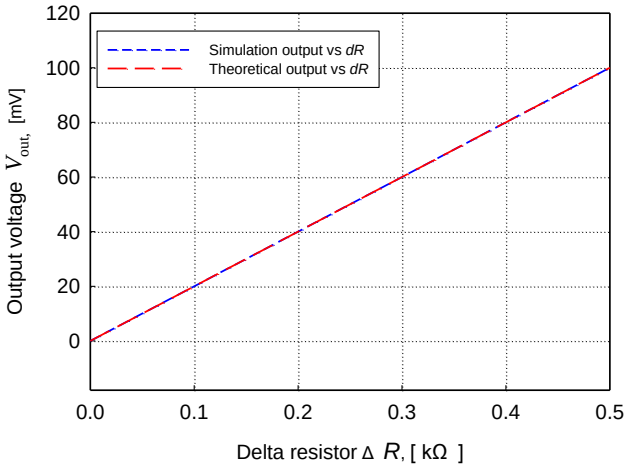

Figure 11. Characteristics of proposed resistance-difference to voltage converter when ΔR is 0 to 0.5kΩ

4. Conclusion and future subjects

This novel configuration of resistance difference to voltage conversion (ΔRVC) was designed and verified using OrCAD simulation. The proposed converter has a simple circuit configuration and does not need to match the resistance requirement and has twice the sensitivity when manufactured in a single semiconductor chip. This resistance difference voltage converter can be realized in a low-cost and a high-precision. In the future, we will optimize the CMOS V-I converter and op-amp by using the fabrication model parameters of 0.18μm Magna/hynix CMOS process and fabricate chip.

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