Self-clock generating TDC for Single-Slope Analog-to-Digital Converter

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Abstract: We propose that Time to Digital converter (TDC) and Ring oscillator are unified into one circuit. And encoder is modified for proper operation. The structure reduce size. By Unifying two circuit and modifying encoder. The encoder also provide reliability. Our work is based on 0.35um process and Virtuoso schematic simulator. Proposed circuit consists of 5-bit TDC and 8-bit counter.

1. Introduction

Their operation is that Sample and Holder locks arbitrary input signal value. The comparator receives ramp signal and signal from sample and holder. It distinguishes which signal is higher. The counter operates until these signals are same. Single-slope ADCs are widely used for column-parallel ADC of CMOS image sensors. Figure 1 and 2 show a block diagram of the conventional Single-Slope ADC.They need smallest area and low complexity. According to progress of image sensors and signal. Industries try to develop ADC with high conversion rate. One of disadvantage of these ADC is long operation time for high conversion rate. A multi-ramp ADC and TDC are solution for conversion speed problem. However, Multi ramp ADC is difficult to generate operating signals. The other way is ADC using TDC. A TDC provide wider resolution. One of disadvantage of TDC is the more resolution raises, the larger size is required. So its resolution is limited. Many of single slope ADCs using TDC connected a counter with the back of Delay line to reduce size. A TDC need a generator to make specific signal and encoder using thermo code[3][4]. Many TDC use an encoder due to a difficulty of signal generator design[1]. Though invertor based TDCs provide doubled resolution, it must generate two start signals at the same time. For this reason, Proposed circuit is buffer based TDC.

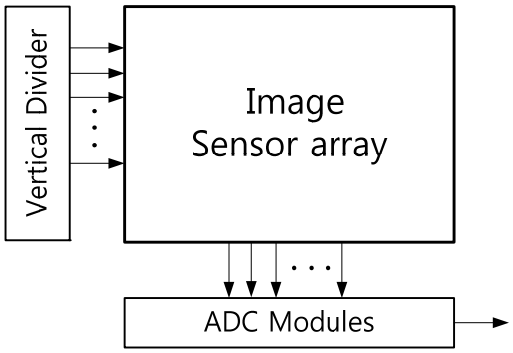


Fig. 1. Block diagram of image sensor module

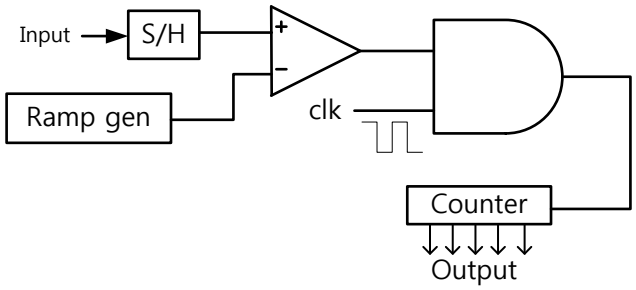


Fig. 2. Hardware strucure of conventional Single-Slope ADC

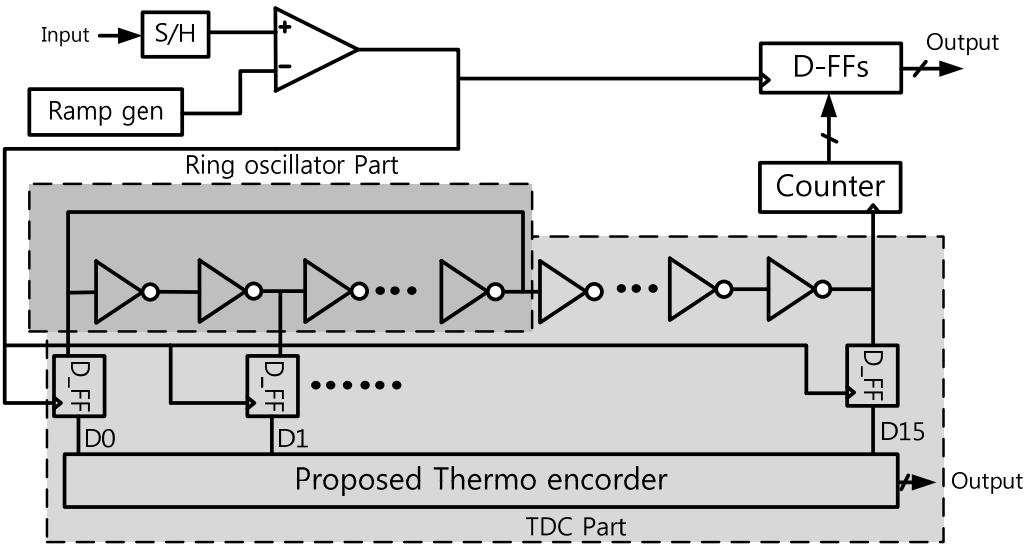


Fig. 3. Proposed TDC for ADC

2. Structure

2.1 Configuration of proposed circuit

A ring oscillator is well known as one of simplest oscillator. The useful feature provide robustness from external disturbances, high oscillation, Wide tuning range and convenience for tuning, It can be easily adopt the latest semiconductor technology. A Ring oscillator consists of odd number of invertors. The output of last invertor is fed back into the first one.

The simple structure of ring oscillator is similar to a delay line based TDC. Figure 3 show diagram for proposed circuit is that even number of invertors and first invertor connect with the middle of inverter in delay line to operate as ring oscillator. The ratched D-FlipFlops(simply called "D-FF") to capture signal from ring oscillator part are placed between each two invertors. And output of every D-FF connects proposed encoder. If place of the encoder and D-FF are exchanged. The time to convert signals from delay line is too short. D-FFs capture delay line signals by the comprator output. A counter connect to last of delay line to provide resolution.

2.2 Delay line Analysis

Proposed circuit mainly consists of invertors for delay. The Invertors from first to the middle of delay line is for Ring oscillator. Whole invertors operate as TDC. The frequency of the ring oscillator is depended on propagation delay τ_d and the number of invertors for ring oscillator n[2]. The frequency of ring oscillator can be expressed as follows:

$$f_{osc} = \frac{1}{2n\tau_d}$$

The propagation delay of invertors is determined by Complementary metal–oxide–semiconductor (simply called "CMOS") parameters. The propagation delay means that

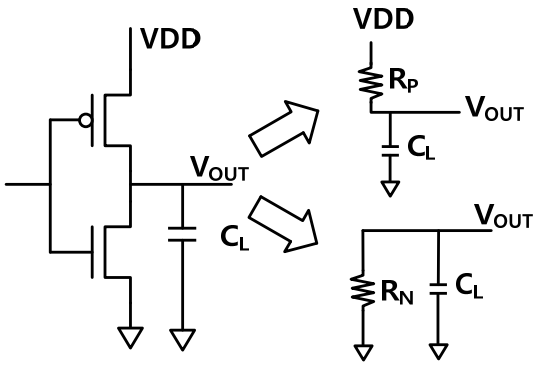


Fig. 4. Block diagram of image sensor module

output change to $V_{DD}/2$ when coming input indicating the other logic. An inverter composes of the n-channel metal oxide semiconductor (NMOS) and the p-channel metal oxide semiconductor (PMOS). PMOS and NMOS in inverter work contrarily. Figure 4 show timing model for inverter. Output response for falling is given by where R_N is an effective resistance of NMOS[5].

$$V_{out}(t) = V_{DD}e^{-t/R_N C_L}$$

Output response for rising is given by where R_P is an effective resistance of PMOS.

$$V_{out}(t) = V_{DD}(1 - e^{-t/R_P C_L})$$

Both cases, the 50% point occurs at

$$\tau = 0.69RC_L$$

Figure 5 show simple inverter model. So we consider two cases:

1) The propagation time τ_{PHL} is falling delay time
2) The Propagation time τ_{PLH} is rising delay time.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Q3	Q2	Q1	Q0	NUM
1	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	0	0	0	0	0
X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	0	0	1	1
X	X	X	X	X	X	X	X	X	X	X	0	0	1	1	X	0	0	1	0	2
X	X	X	X	X	X	X	X	X	X	0	0	1	1	X	X	0	0	1	1	3
X	X	X	X	X	X	X	X	X	0	0	1	1	X	X	X	0	1	0	0	4
				• • •		• • •		• • •		• • •		• • •		• • •						
X	X	0	0	1	1	x	x	x	x	x	x	x	x	x	x	1	0	1	1	11
X	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	1	1	0	0	12
0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	1	1	0	1	13
0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	0	1	1	1	0	14
1	1	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	1	1	1	15

Table 1. Modified thermo encoder

Frequency of ring oscillator can be more accurately expressed as follows:

$$f_{\text{osc}} = \frac{1}{\text{n}(\tau_{PHL}+\tau_{\text{PLH}})}$$

Parasitic effect and nonlinearities of circuit make calculation difficult. We can get the propagation delay time by using simulation. If T is period of signal from ring oscillator, the propagation delay can be expressed as follow:

$$\tau_{\text{d}} = \frac{\text{T}}{n}$$

To control period for ring oscillator, We consider changing inverter size. Power consumption of ring oscillator is proportional to frequency. To reduce frequency, size of inverters need to be wider.

2.3 Modified Thermo Encoder

A TDC without a encoder needes generator making very nallow signal. The signal must be proper for Delay line and D-FF. however, The thermo code is to detect the pulse duration of square wave[3][4]. The encoder for TDC ditinguish how long signal pass through. Proposed encoder only detect rising edge. Table 1 show the true table. Each output of proposed encoder can be expressed as follow:

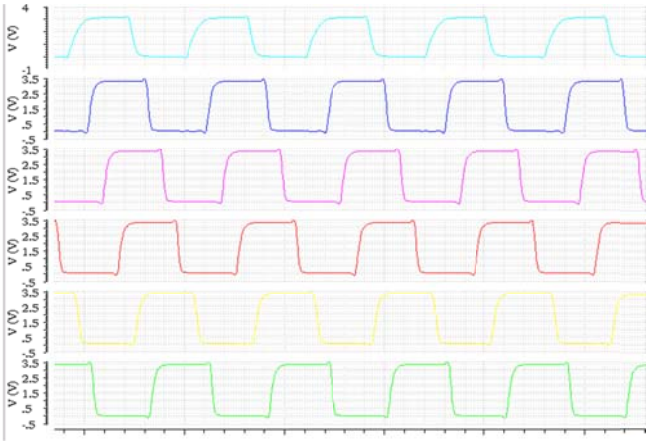
$$\begin{aligned} Q_0 = {} & \sum B3 \cdot B2 \cdot D1 \cdot D0 + B5 \cdot B4 \cdot D3 \cdot D2 \\ & + B9 \cdot B8 \cdot D7 \cdot D6 + B11 \cdot B10 \cdot D9 \cdot D8 \\ & + B13 \cdot B12 \cdot D11 \cdot D10 + B15 \cdot B14 \cdot D13 \cdot D12 \\ & + B1 \cdot B0 \cdot D15 \cdot D14 \end{aligned}$$

$$\begin{aligned} Q_1 = {} & \sum B4 \cdot B3 \cdot D2 \cdot D1 + B5 \cdot B4 \cdot D3 \cdot D2 \\ & + B8 \cdot B7 \cdot D6 \cdot D5 + B9 \cdot B8 \cdot D7 \cdot D6 \\ & + B12 \cdot B11 \cdot D10 \cdot D9 + B13 \cdot B12 \cdot D11 \cdot D10 \\ & + B1 \cdot B0 \cdot D15 \cdot D14 \end{aligned}$$

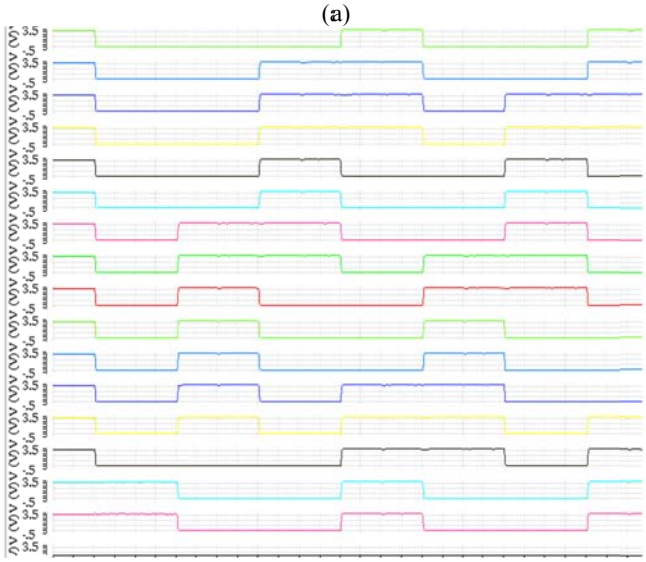
$$\begin{aligned} Q_2 = {} & \sum B6 \cdot B5 \cdot D4 \cdot D3 + B7 \cdot B6 \cdot D5 \cdot D4 \\ & + B8 \cdot B7 \cdot D6 \cdot D5 + B9 \cdot B8 \cdot D7 \cdot D6 \\ & + B14 \cdot B13 \cdot D12 \cdot D11 + B15 \cdot B14 \cdot D12 \cdot D11 \\ & + B1 \cdot B0 \cdot D15 \cdot D14 \end{aligned}$$

$$\begin{aligned} Q_3 = {} & \sum B10 \cdot B9 \cdot D8 \cdot D7 + B11 \cdot B10 \cdot D9 \cdot D8 \\ & + B12 \cdot B11 \cdot D10 \cdot D9 + B13 \cdot B12 \cdot D11 \cdot D10 \\ & + B14 \cdot B13 \cdot D12 \cdot D11 + B15 \cdot B14 \cdot D12 \cdot D11 \\ & + B1 \cdot B0 \cdot D15 \cdot D14 \end{aligned}$$

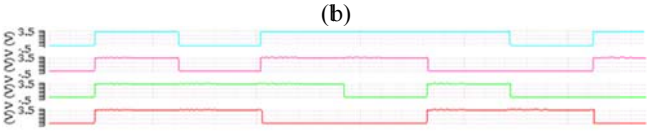
where D is D-FF output and B is output of inversed D-FF. The equations above show encorder logics. The encoder can be easily simplified using this chracteristics. so Proposed encoder requires less chip area compared with conventional encoder. Because conventional thermo encoder needs more OR gates to detect entire pulse duration of square wave.



(a)



(b)



(c)

Fig. 6. (a) Signal in delay line. (b) Response of D-FFs of TDC. (c) TDC binary output

3. Simulation result

The simulation for proposed circuit is limited to the TDC and ring oscillator. Our simulation is based on 0.35μm process technology. Figure. 6(a) show samples of every two inverters in delay line. The period of signal ring oscillator is nearly 20ns. Each inverter make signal delay nearly 1.2ns. Figure. 6(b) show part of D-FFs output by arbitrary control signal. The control signal is virtual comprator output of single slope ADC. Almost half of D-FF output is high. The others are low. Conventional encoder using thermo code need to completly match True table. Proposed encorder only detect rising edge of signal in delay line. Figure. 6(c) is output of encoder. Figure. 6(b) and figure. 6(c) show the results are at the same time

4. Process realization

We propose TDC and Ring oscillator part. Figure .6 show Proposed TDC operate properly in simulation with Virtuoso Schamatic simulater. We plan to unify the TDC and part of ADC in progress. This work is based on 0.35um process. we plan to adopt advanced simeconductor process for simulation. It can not be controlled by outside signal. We need to test operation of ring oscillator many times. One of disadvantage of our ring oscillator is unconrtollable delay time. To control delay time, We will adopt Variable Control Delay Line[6] or other technologies[7].

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