Combinational Logic Computing for Single-Flux Quantum Circuits with Asynchronous Collision-Based Fusion Gates

Kazuhito Yamada, Tetsuya Asai, and Yoshihito Amemiya

Graduate School of Information Science and Technology, Hokkaido University
Kita 14, Nishi 9, Kita-ku, Sapporo 060-0814, JAPAN
Email: k_yamada@sapiens-ei.eng.hokudai.ac.jp

Abstract—We propose a single-flux-quantum (SFQ) logic system based on the reaction-diffusion-collision fusion computation. The fusion computation is a way of digital processing that performs logic operation by applying analogy of nonlinear physical and chemical systems to the structure of the logic operation. It is very powerful for implementing a given digital operation with a small number of logic gates. A fusion computation system consists of regularly arrayed unit cells, where each cell has two input arms and two output arms and is connected to its neighboring cells with the arms. Each cell accepts two input signals A and B and produces two output signals $A\overline{B}$ and $\overline{A}B$. A fusion computation system, as a whole, can operate any combinational logic function. We designed functional SFQ circuits that implemented the fusion computation. The unit cell was able to be made with ten Josephson junctions. Circuit simulation showed that SFQ fusion computation systems could operate at very high speed, about ten times faster than conventional CMOS logic systems.

1. Introduction

Collision-based computing, which was originally introduced in conservative computation such as a billiard-ball model [1] and its cellular-automaton (CA) analogues [2], presents a novel approach of computation with mobile physical objects (e.g., billiard balls), chemical particles, self-localized patterns on CAs, and so on. Although a number of mathematical and abstract models have been proposed [3], the physical (LSI) implementation is still difficult because i) collision-based physical models require conservative media for series computation and ii) CA systems have to implement complex rules per a cell for producing self-localized patterns. Collision-based fusion gates, which fuse billiard-ball models and excitable properties of chemical waves in reaction-diffusion media [4], have recently been proposed as a possible solution to LSI implementation of collision-based computers [3, 5, 6]. The fusion computing is a way of digital processing that performs logic operation, and is very powerful for implementing a given digital operation with a small number of logic gates [6]. Therefore, in [7], we have proposed single-flux-quantum (SFQ) circuits to construct fusion-computing circuits for combinational logic processing.

In collision-based (fusion) computing, information propagates in an impulse form; i.e., existence of a mobile object, particle or self-localization is represented by a spatial impulse on the abstract media. Unlike other electronic devices, a medium for signals in SFQ circuits is a pulse of a fluxoid quantum, therefore SFQ circuits are able to implement the collision-based computers more simply. However, there exists two severe problems on implementing fusion computing as well as collision-based computing: i) collision timing control of impulses and ii) expression of logical '0' in impulse forms. In this report, we show possible solutions to these problems by introducing dual-rail representation of data.

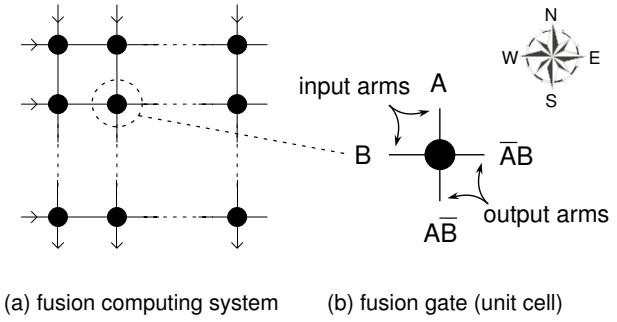


Figure 1: Fusion computing systems.

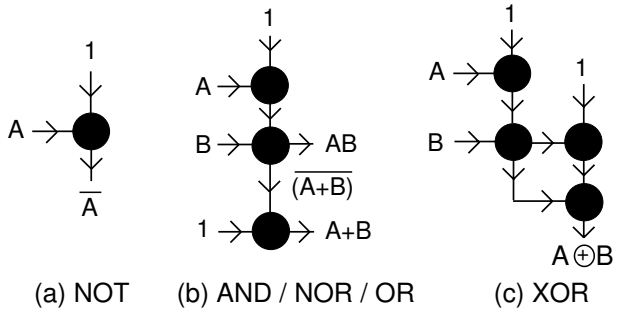


Figure 2: Examples of logic computing in fusion computing systems.

2. Logic computation with fusion gates

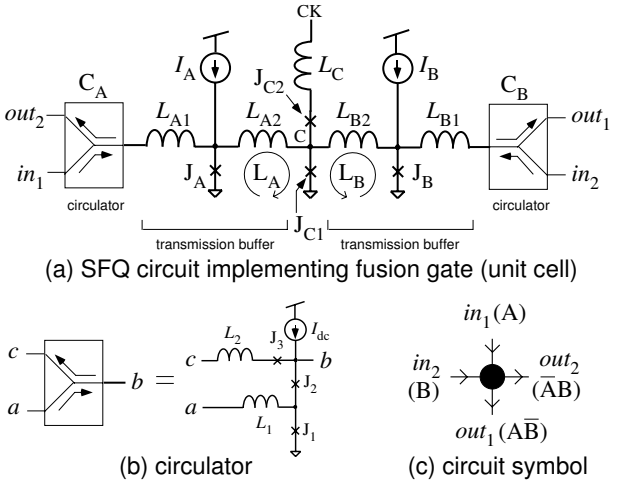
A fusion computation system consists of regularly arrayed unit cells (fusion gates) where each cell has two input arms and two output arms and is connected to its neighboring cells with the arms (Fig. 1). A unit cell accepts two logic inputs from its North and South arms, and outputs two logic signals to the East and South arms. The cell's inputs are represented by logical variables A and B where A (or B) = '1' represents the existence of an impulse train traveling North-South (or West-East), and A (or B) = '0' represents the absence of impulse trains. When A = B = '1' we assume that impulses collide at the center position (black circle) and then disappear, as observed in excitable chemical waves on reaction-diffusion media [2, 4]. East and South outputs are thus '0' because of the disappearance. If A = B = '0', the outputs will be '0' as well because of the absence of the impulses. When A = '1' and B = '0', an impulse given at the north node (A) can travel to the South because it does not collide with an impulse traveling West-East. The East and South outputs are thus '0' and '1', respectively, whereas they are '1' and '0', respectively, when A = '0' and B = '1'. Consequently, output logical functions of this simple 'gate' are represented by $A\overline{B}$ and $\overline{A}B$ ($\overline{A}$ and $\overline{B}$ represent logical negation of A and B, respectively). We call this unit a 'fusion gate' that utilizes properties of collision-based kinetics and excitable waves.

Figure 2 represents basic logic circuits constructed by combining several fusion gates. The simplest example is shown in Fig. 2(a) where the NOT function is implemented by a single fusion gate. The North input is always '1', whereas the West is the input (A) of the NOT function. The output appears on South node ($\overline{A}$). Figure 2(b) represents a combinational circuit of three fusion gates that produces AND, NOR, and OR functions simultaneously. Exclusive logic functions (XOR and XNOR) are constructed by three fusion gates as shown in Fig. 2(c). Any combinational circuit can be constructed by combining fusion gates [5, 6].

3. Fusion device consisting of SFQ circuits

We designed functional SFQ circuits that implemented the fusion gate [7]. Figure 3 shows the unit cell consisting of two circulator circuits and two transmission buffers including two memory loops (L_A and L_B).

A circulator consists of three Josephson junctions J_1-J_3, and two inductances L_1 and L_2 biased by a constant current I_{dc}, as shown in Fig. 3(b). Let I_i and I_{sfq} denote the critical current of J_i and the loop current of an SFQ, respectively. When $I_1 < I_{sfq} + I_{dc}$, $I_3 > I_{sfq}$ and $I_2 < I_{sfq} + I_{dc}$, an input SFQ pulse given to node '*a*' is transmitted to node '*b*' because J_1 (and then J_3) is switched to a resistive state. On the other hand, a pulse given to node '*b*' is not transmitted to node 'a' because J_2 (and then J_3) is switched to a resistive state. An input SFQ pulse given to node '*a*' is not transmitted to node '*c*' because the SFQ current of J_2



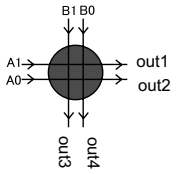
(a) SFQ circuit implementing fusion gate (unit cell)

(b) circulator (c) circuit symbol

Figure 3: SFQ circuits for synchronous fusion gate.

branches to J_3 and node '*b*', and the branched current to J_3 is faded away when J_3 is switched to a resistive state. Contrary, an input SFQ pulse given to node '*b*' is transmitted to node '*c*' with this condition because J_2 is switched to a resistive state and the SFQ current is directly flowing into J_3 (J_3 is then switched to a resistive state by this non-branched current). Therefore this circuit transmits flux quanta from node '*a*' to '*b*' and from '*b*' to '*c*' only.

In Fig. 3(a), when a SFQ pulse is applied to node in1 only (A = '1' and B = '0'), it propagates to center node *C* via circulator C_A and a transmission buffer (L_{A1}, L_{A2}, J_A and I_A). When clock node CK was set at '0', the SFQ is stored in Josephson memory loop L_A. When a voltage clock pulse is applied to CK, the stored SFQ is transmitted to circulator C_B and is sent to out_1. It should be noted that this processing requires one clock step. Similarly, when A = '0' and B = '1' (a SFQ pulse is applied to node in_2 only), the input SFQ is transmitted to out_2 only. When A = '1' and B = '1', the sum of SFQ currents in loops L_A and L_B exceed the critical current of J_{C1}. Therefore the SFQs in L_A and L_B fade away, and no SFQs are transmitted to out_1 and out_2. When A = '0' and B = '0', no SFQ outputs are generated at out_1 and out_2. Consequently, representing the existence and absence of SFQ pulses at



A	B	A1	A0	B1	B0	out1	out2	out3	out4
0	0	0	1	0	1	0	1	0	1
0	1	0	1	1	0	0	1	1	0
1	0	1	0	0	1	1	0	0	1
1	1	1	0	1	0	0	1	0	1

Figure 4: Proposed dual-rail fusion gates.

input and output nodes by logical variables, this circuit computes A$\overline{B}$ and $\overline{A}$B from inputs A and B. Fig. 3(c) illustrates the circuit symbol and the correspondence between the circuit nodes and the input-output logics.

4. Asynchronous Fusion device consisting of SFQ circuits

In CMOS fusion computing systems, we used continuous voltages to represent the input and output logic values, instead of a single voltage pulse, without using any timing control circuits [5, 6]. The same strategy could be used in SFQ circuits if we utilize multiple-flux-quantum switching properties in Josephson junctions. However, the present SFQ fusion gate [7] requires clocks and memory buffers for the timing control. This means, if the number of fanout paths were increased, the time required for obtaining the final results is also increased. A possible solution to this problem is to eliminate the synchronous timing control circuitry and to use asynchronous dual-rail structures to represent the input and output logic values. Figure 4 shows dual-rail representation of a single fusion gate. Since both logical '0' and '1' are represented by the existence of SFQ pulses, one can here employ an asynchronous computing structure as in conventional SFQ circuits. When both the inputs (A and B) have arrived at a fusion gate, a drive signal is produced by itself to emit the output. Figure 5 shows the basic simulation results of asynchronous fusion gates with standard Nb/Al-AlOx/Nb 2.5-kA/cm^2 process parameters. Four combinations of logical inputs were given to the gate. The fusion gate produced the expected outputs asynchronously. The maximum delay time

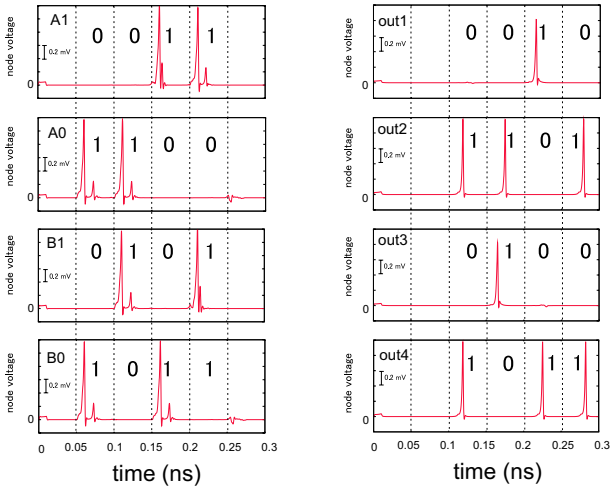


Figure 5: Simulation results of SFQ networks implementing dual-rail fusion gates.

was about 50 ps, which implies that the proposed circuit can cope with synchronous SFQ circuits operating at 20 GHz clock, although the maximum clock frequency of present SFQ circuits in [7] was 10 GHz.

Acknowledgments

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