

# A 0.18um CMOS Current Reused Low-Noise Amplifier with Gain Compensated for Ultra-Wideband Wireless Receiver

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**Abstract** - A current reused low-noise amplifier (LNA) with gain compensated to extend the bandwidth and is designed for ultra-wideband (UWB) wireless receiver. The design consists of two cascode common-source amplifier and an output buffer which is implemented in 0.18um RF CMOS process. The LNA gives 13.1dB gain; 9.1GHz 3dB bandwidth (3.1-12.2GHz) while consuming 13.9mW through a 1.8V supply. Over the 3.1GHz - 10.6GHz frequency band, a minimum noise figure of 2.7dB and input return loss lower than -8.7dB have been achieved.

**Index Term** - RFIC, Ultra-Wideband, UWB, Gain Compensated, Current Reused, LNA and Low-Noise Amplifier.

## I. INTRODUCTION

Since the approval of the ultra-wideband (UWB) radio technology for low power wireless communication application in February, 2002, [1] UWB systems has become an increasingly popular technology which is capable of transmitting data over a wide spectrum of frequency with very low power and high data rate. Although the IEEE UWB standard (IEEE 802.15.3a [2]) has not been completely defined, two major proposed solutions, MB-OFDM and DS-UWB, are all allowed to transmit in a band between 3.1GHz-10.6GHz and 3.1GHz-9.6GHz. The band definition of MB-OFDM is illustrated in Fig.1 (a) which extended from 3176MHz to 10552MHz and the band definition of DS-UWB are from 3100MHz to 4900MHz and 6000MHz to 9700MHz. The bandwidth of MB-OFDM is containing Group-1, Group-3, Group-4 and Group-5. Group-2 is not considered in current UWB system which caused by the U-NII band and WLAN (IEEE 802.11a). The bandwidth of DS-UWB is with Low-Band and High-Band which is in Fig.1 (b).

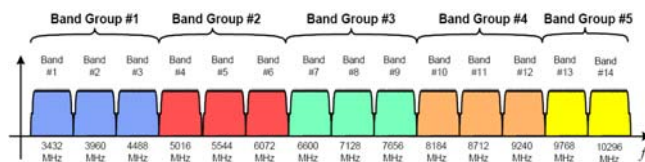


Fig.1 (a) Band Groups of MB-OFDM

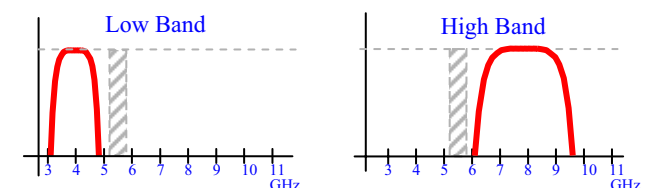


Fig.1 (b) Low Band and High Band of DS-UWB

In RF wireless receiver, LNA is one of the most critical building blocks caused by the noise figure is dominated in 1<sup>st</sup> stage of the receiver that is illustrated in Fig. 2. For LNA design, there are many trade-off between different specifications. For example, the power gain affects noise figure, the die area affect cost, and the power consumption affects the battery life. This paper is focused on the design and implementation of the UWB specifications; the low-noise amplifier for ultra-wideband receiver is implemented in a 0.18um Standard RF CMOS Process.

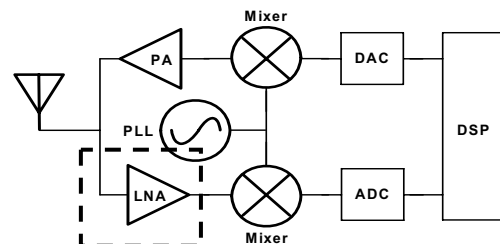


Fig.2 UWB Transceiver Architecture of MB-OFDM

## II. DESIGN OF ULTRA-WIDEBAND LNA

### A. Wideband Amplifier Design

A simple figure of the wideband amplifier which contains input matching network, main amplifier and output buffer and that is shown as Figure 3. The specification of ultra-wideband system is defined as 3.1GHz-10.6GHz, therefore a very wide bandwidth input matching network is necessary in the UWB LNA. For measurement consideration, the output impedance is always designed for 50 ohms in the output buffer. The design considerations of low-noise amplifier are mainly in input return loss, power gain, and noise figure (NF), linearity (P1dB, IIP3) and power consumption, but there are some trade-off between these important characteristics.

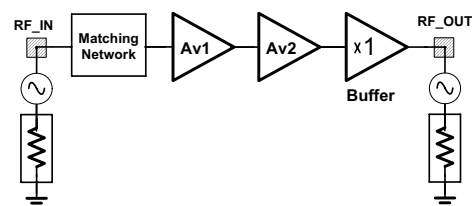


Fig.3 Wideband Amplifier Design

### B. Wideband Input Impedance Matching

Wideband input impedance matching is a critical design challenge in ultra-wideband system. Some excellent wideband input impedance matching solutions are proposed in [3]. The wideband input impedance matching network including the conventional source-degeneration input matching and an inductor shunted in input RF path which is shown in Fig. 4; both of the circuits contribute one resonated frequency  $f_{r1}$  and  $f_{r2}$  to extend the bandwidth of the input matching. Equation (1) is the total equivalent input impedance  $Z_{in}$ , where  $L_g$ ,  $L_s$ ,  $L_m$  are gate inductor, source inductor and matching inductor,  $C_{gs1}$  is the parasitic capacitor in MOS transistor and  $\omega_r$  is the unity gain frequency of the transistor.

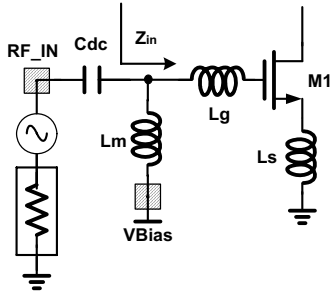


Fig. 4 Input Impedance Matching Network

$$Z_{in} = \frac{s^2 L_m L_g C_{gs1} + s \omega_r L_m L_s C_{gs1} + L_m}{s^2 L_g C_{gs1} + s(\omega_r L_s C_{gs1} + L_m C_{gs1}) + 1} \quad (1)$$

### C. Cascoded Amplifier with LC-Tank Load

The most popular topology of low-noise amplifier is cascode amplifier with LC tank, as illustrated in Fig. 5(a), which eliminates the Miller effect on input transistor to achieve high-frequency performance. The load with LC-tank is mostly used in narrow-band systems due to its excellent frequency-selective characteristics that are shown as Figure 5(b). And the voltage gain  $A_{L1}$  of this low-noise amplifier is expressed in equation (1), where  $g_{m1}$  is the transconductance of the MOSFET,  $r_{o1}$ ,  $r_{o2}$  are the output impedance of the transistors, and inductor  $L$ , capacitor  $C$  are the load of the LC-tank.

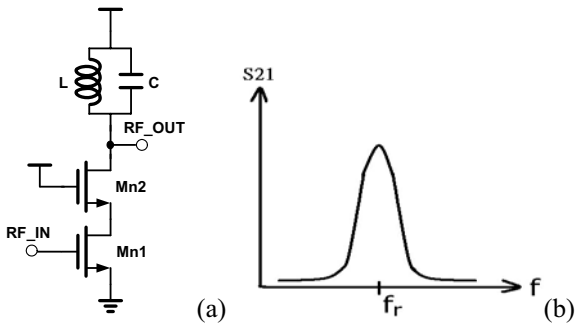


Fig. 5 Cascode LNA with LC-tank (a) and Power Gain (b)

$$A_{L1} \approx -g_{m1} \cdot \frac{s g_{m2} r_{o1} r_{o2} L}{s^2 g_{m2} r_{o1} r_{o2} LC + sL + g_{m2} r_{o1} r_{o2}} \quad (2)$$

### D. Cascade Amplifier with LC-Tank Load

Therefore, two stages of LC-tank resonated amplifiers could achieve higher power gain and wider bandwidth; as shown in Fig.6. The first stage amplifier with LC-tank resonated loading is providing the power gain of lower frequency, and the second stage amplifier is providing the power gain of the higher frequency, which are the blue dash lines in Fig. 7; the resonated center frequency are  $f_{r1}$  and  $f_{r2}$ . And final power gain of the low-noise amplifier is the red solid line in Fig. 7 which is the result of two stage amplifiers in gain compensated; the wide bandwidth is produced.

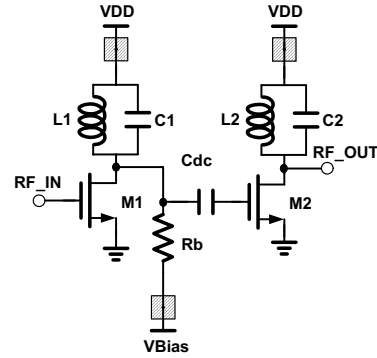


Fig.6 Cascade Common-Source Amplifiers

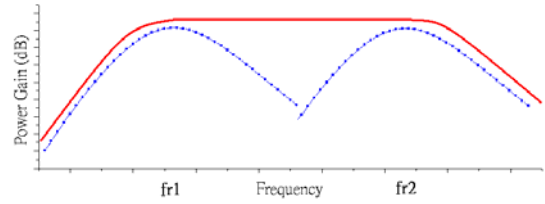


Fig.7 Gain Compensation

### E. Proposed UWB Low-Noise Amplifier

The proposed UWB low-noise amplifier is shown in figure 8 which consists of the input matching network that is implemented by the Butterworth Filter [3] where are  $L_m$ ,  $L_g$ ,  $L_s$  and  $C_{gs1}$ ; the main amplifier is containing  $M_1$ ,  $M_2$ ,  $L_1$ , and  $L_2$ ; the output buffer is the  $M_3$ ; the  $C_{dc}$  are DC blocking capacitors and  $C_{ac}$  is AC ground capacitor. The first stage amplifier  $M_1$  contributes the lower frequency power gain; the RF signal ends at  $C_{ac}$  capacitor, but also travels to  $C_{dc}$  path. Then the second stage amplifier  $M_2$  contributes the higher frequency power gain. The DC current flows through transistors  $M_1$  and  $M_2$ ; therefore, the DC current is saved and the power dissipation is also saved. The inductor  $L_{sp}$  is a series peaking inductor, and the power gain in frequency response is extended which is shown in Fig.9; the input return loss is also influenced by this series peaking inductor which dues to the bad isolation of the common-source amplifier that is also shown in Fig. 10. The inductor also reduces the gate noise in higher frequency from the MOSFET  $M_2$ ; the comparison is also available in Fig. 11.

### III. SIMULATION RESULTS

The simulation results of the proposed UWB LNA using Agilent ADS 2006A simulator are given in Figure 12 to Figure 17. In Figure 12 that can be seen the input return loss (S11) are lower than -8.7dB between 3.1GHz to 10.6GHz. In Figure 12, that can be seen that the output return loss (S22) are lower than -10.9dB between 3.1GHz to 10.6GHz, respectively. The power gain whose peak value is 13.1dB at 9.5GHz and which is shown in Figure 14. In Fig. 15, it can be seen that the noise figure is below 4.9dB between 3.1GHz to 10.6GHz and the minimum noise figure are 2.7dB at 4.3GHz through 1.8V supply voltage. The input-referred 1dB compression point (IP1dB) is -19dBm at 7.0GHz which is in Fig. 16. In figure 17, the Third-Order Input Intercept Point (IIP3) at 6336MHz and 6346MHz is -9dBm. The power consumption is 13.9mW through 1.8V supply voltage which neglects the power of output buffer.

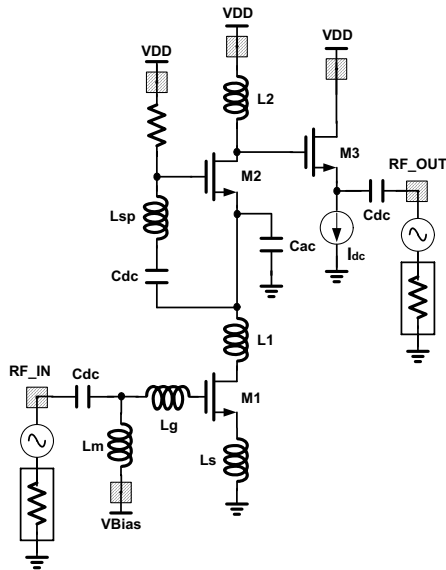


Fig. 8 Proposed UWB Low-Noise Amplifier

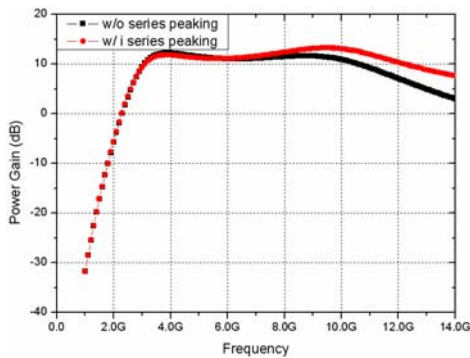


Fig. 9 Power Gain w/o and w/i Series Peaking

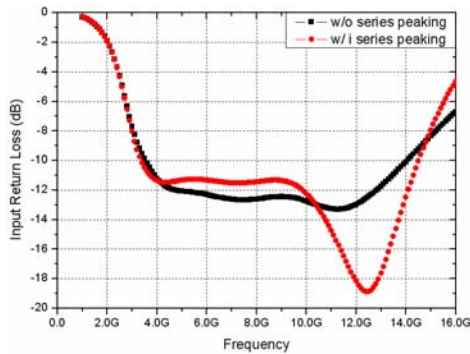


Fig. 10 Input Return Loss w/o and w/i Series Peaking

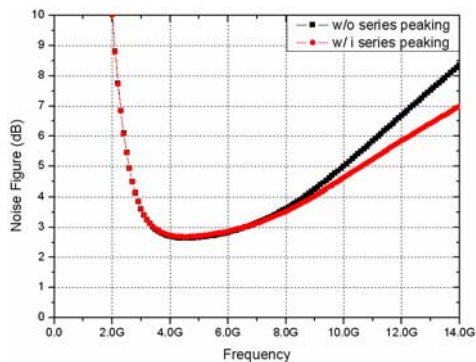


Fig. 11 Noise Figure w/o and w/i Series Peaking

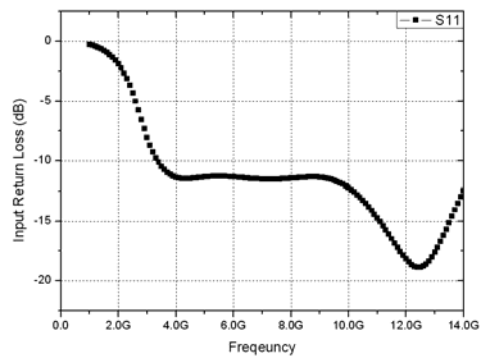


Fig. 12 Input Return Loss (S11)

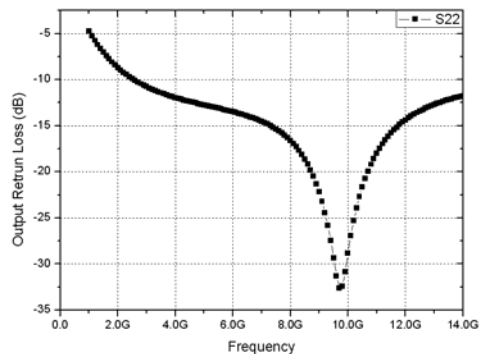


Fig. 13 Output Return Loss (S22)

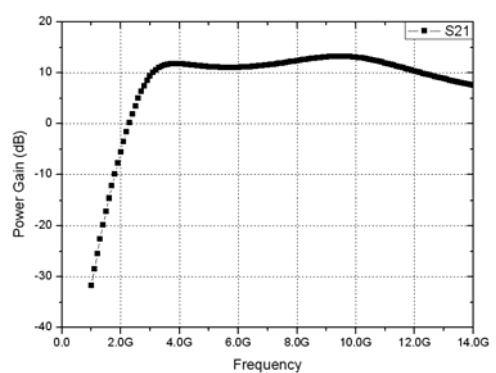


Fig. 14 Power Gain (S21)

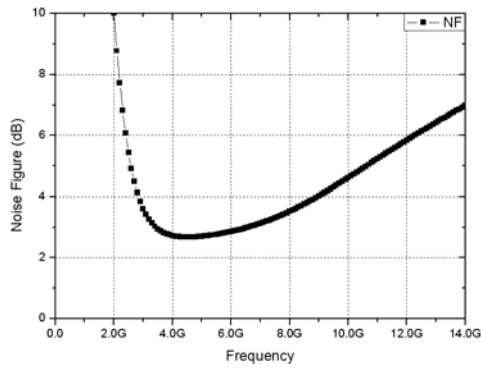


Fig. 15 Noise Figure

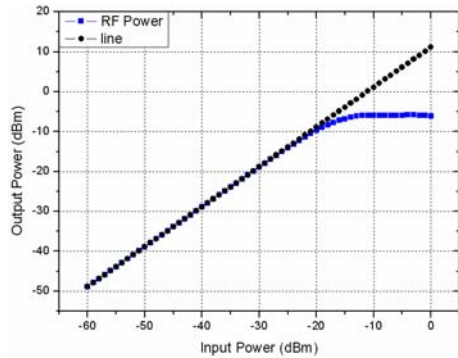


Fig. 16 Input-Referred 1dB Compression Point (P1dB)

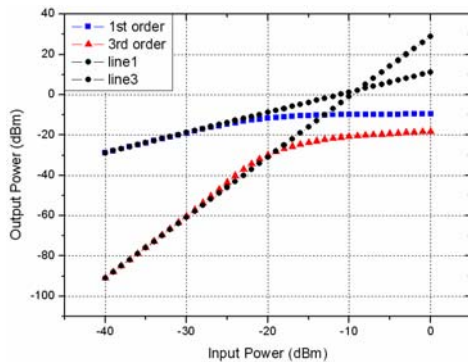


Fig. 17 Third-Order Input Intercept Point (IIP3)

#### IV. CONCLUSIONS

A CMOS UWB LNA is designed with current reused technic for ultra-wideband wireless system; the bandwidth extended from 3.1GHz to 10.6GHz. The simulation results show that the proposed LNA gives 13.1dB power gain for 3.1-10.6GHz, 9.1GHz 3dB bandwidth (3.1-12.2GHz) while consuming 13.9mW through 1.8V power supply. Over the 3.1GHz - 10.6GHz frequency band, a minimum noise figure of 2.7dB have been achieved.

Table.1 Performance Conclusions

|                         |             |
|-------------------------|-------------|
| S11 (dB)                | < -8.7      |
| S22 (dB)                | < -10.9     |
| S21 (dB)                | 10.0 ~ 13.1 |
| S21 Max. (dB)           | 13.1        |
| Working Bandwidth (GHz) | 3.1 ~ 10.6  |
| 3dB Bandwidth (GHz)     | 3.1 ~ 12.2  |
| NF (dB)                 | 2.7 ~ 4.9   |
| NFmin (dB)              | 2.7         |
| IP1dB (dBm)             | -19         |
| IIP3 (dBm) [10MHz]      | -9          |
| Power Consumption (mW)  | 13.9        |

#### ACKNOWLEDGMENT

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Table.2 Comparison of the Proposed UWB LNA with Other Reported Wideband LNA

| Paper     | Circuit Topology      | Technology  | S11(dB) | S22(dB) | S21(dB)   | BW(GHz)  | Gmax(dB) | NF(dB)  | NFmin(dB) | Pdiss(mW) |
|-----------|-----------------------|-------------|---------|---------|-----------|----------|----------|---------|-----------|-----------|
| [4]       | resistive feedback    | 0.18um CMOS | < -9    | < -10   | 6.8-9.8   | 2.0-4.6  | 9.8      | 2.3-5.2 | 2.3       | 12.6      |
| [5]       | 3-stages comm.-source | 0.18um CMOS | < -12.2 | < -10.1 | 13.5-15.8 | 3.0-6.0  | 15.76    | 4.7-6.7 | 4.7       | 59.4      |
| [6]       | 3-stages shunt-peaked | 0.18um CMOS | < -7    | < -12   | 6.7-9.7   | 1.2-11.9 | 9.7      | 4.5-5.1 | 4.5       | 20.0      |
| [7]       | 2-stages comm.-source | 0.18um CMOS | < -8.7  | < -9.2  | 9.0-12.0  | 3.0-11.0 | 12.0     | 4.2-7.6 | 4.2       | 7.3       |
| This Work | Current reused        | 0.18um CMOS | < -8.7  | < -10.9 | 10.0-13.1 | 3.1-12.2 | 13.1     | 2.7-4.9 | 2.7       | 13.9      |