A Design of Low-Power Frequency Synthesizer for GPS Application using Multiple Reference Clocks in 0.18 μm CMOS Technology

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Abstract: This paper presents a low power CMOS frequency synthesizer for GPS application that can support multiple reference clocks. The frequency synthesizer has fractional-N phase locked loop structure with sigma-delta modulator to allow multiple reference clock frequencies. The measured phase noise is -126dBc/Hz at 1MHz offset from the carrier. This chip is fabricated with 0.18μm CMOS technology, and the die area of the frequency synthesizer is 1.1mm x 1.05mm. The power consumption is 18mW at 1.8V supply voltage.

Keywords : frequency synthesizer, low-power, GPS, phase noise

1. Introduction

With the FCC regulation (Enhanced 911), every cellular devices should be capable of determining the location with better than 100-meters accuracy and the related market is demanding low-cost solutions for satellite navigation [1]. The global positioning system (GPS) is dominating the market of satellite navigation. Traditionally, GPS radios were implemented with bipolar technology [2]-[5] and most of the mass products on the market are still using bipolar technology. With the rapid improvement of the RF performance of CMOS technology and the increasing demand of low cost and higher level of integration, the interest on CMOS GPS receiver becomes higher and several successful results have been reported [6]-[7].

In this work, a low-power frequency synthesizer for GPS application that can support multiple reference clocks is developed with a 0.18 μm CMOS technology.

2. Architecture

Figure 1 shows the block diagram of the frequency synthesizer. It is composed of phase frequency detector (PFD), charge pump (CP), voltage controlled oscillator (VCO), prescaler, and Sigma-Delta modulator.

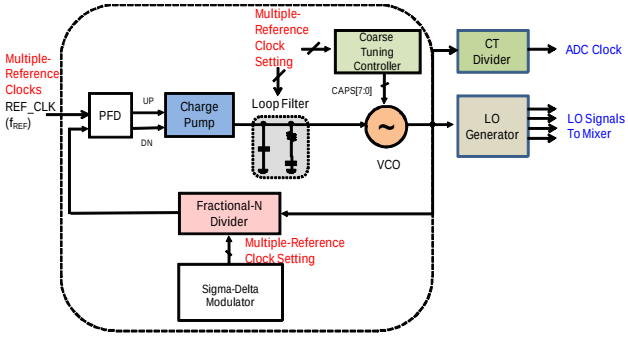

Figure 1. Frequency synthesizer with fractional-N PLL architecture.

To down-convert the L1-band signal centered at 1.575GHz to 4.092MHz IF, the frequency of the local oscillator (LO) signal should be 1.571GHz. Because there is only one channel in GPS, it is possible to use a simple integer-N phase locked loop (PLL) frequency synthesizer to generate the LO. In this work, however, a fractional-N PLL frequency synthesizer is used to allow multiple reference clock frequencies so the dual-mode GPS receiver can share a TCXO with the other RF transceiver coexisting on the same system. According to the reference clock frequency, the fractional division ratio is programmed. At the same time, the optimal resistances and capacitances are selected based on the reference clock frequency.

The ADC clock is generated from the shared coarse tuning divider which is used for the coarse tuning controller to reduce the die area.

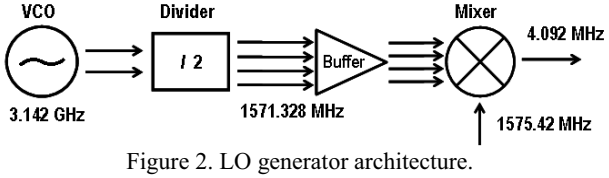

Figure 2. LO generator architecture.

Figure 2 shows the LO generator architecture. The output of the voltage controlled oscillator (VCO) oscillating at 3.142GHz is divided by two to get the 1.571GHz quadrature LO signals.

2. Building Blocks

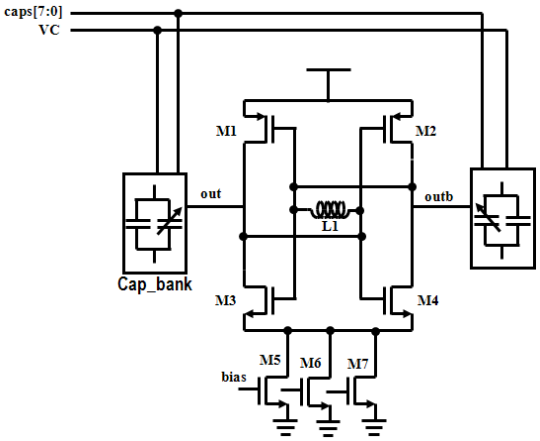

Figure 3. Voltage controlled oscillator.

The LC-type VCO shown in Figure 3 is used to meet the phase noise specification. It is composed of a fixed capacitance, coarse tuning capacitances, and variable capacitance (varactor).

To minimize the phase noise, the gain of the VCO, K_{VCO}, is limited to be smaller than 25MHz/V and to widen the frequency tuning range, 8-bit capacitor bank is used, which is controlled by automatic coarse tuning loop.

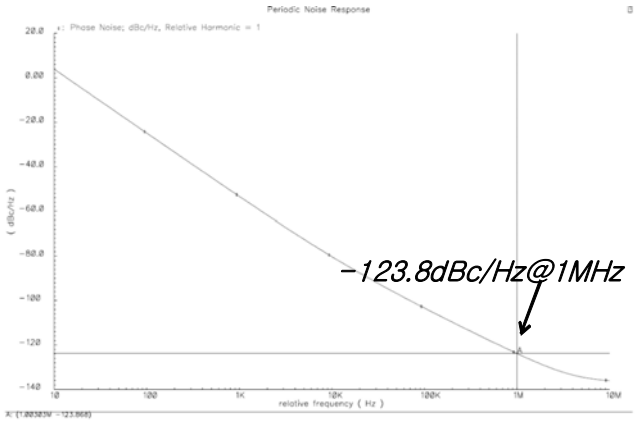

Figure 4. Phase noise simulation result of VCO.

Figure 4 shows the phase noise simulation result of VCO. It is -123dBc/Hz at 1MHz offset.

Charge pump is one of the most important blocks in the performance of frequency synthesizer. It is very important to match up/down currents of the charge-pump. Phase Noise characteristic of the PLL is degraded due to the UP/DOWN current mismatch.

Figure 5 shows the charge pump circuits. In general, the current mismatch can be reduced as the current level is higher. However, the charge pump is designed to have up/down current of 30μA for the low power consumption. The output resistance of the current source should be increased to improve its accuracy and linearity characteristics.

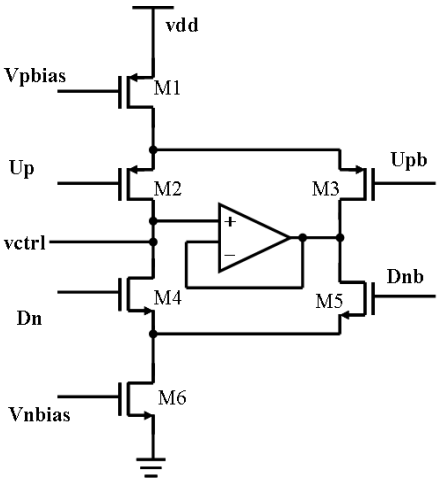

Figure 5. Block diagram of the charge-pump.

Figure 6 shows the DC simulation result of the charge pump to check the linear current range. It is about 1.2V centered at 0.9V

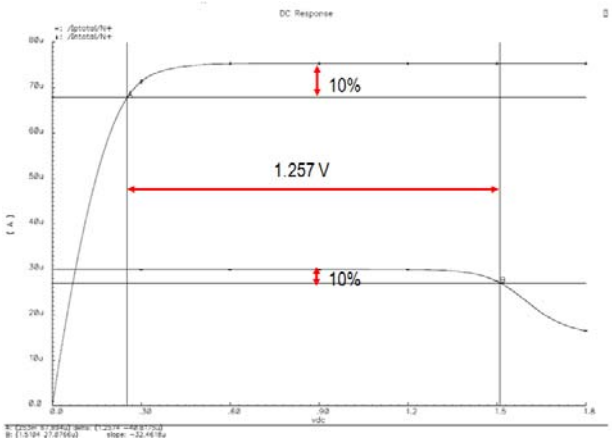

Figure 6. DC simulation result of charge pump.

The low-pass filter (LPF) has a zero and two poles comprising a third-order system. In this design, the LPF is implemented with the resistance and capacitance arrays to support the multiple reference clocks as shown in Figure 7. Third-order loop is adopted to suppress the out-of-band phase noise generated from the sigma-delta modulator.

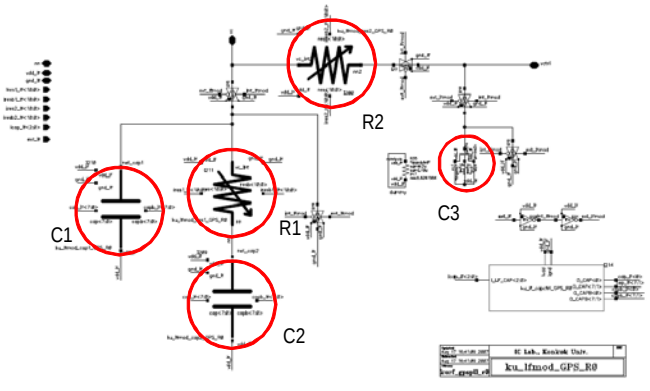

Figure 7. 3rd order Loop Filter.

The dividier-by-2 circuit are used to provide the 1.571GHz clock to the down-conversion mixer. It is implemented with the CML type F/F for high speed operation. The CML circuit used in the divider is shown in Figure 8. It is used in order to be relatively insensitive to supply noise and to minimize power consumption.

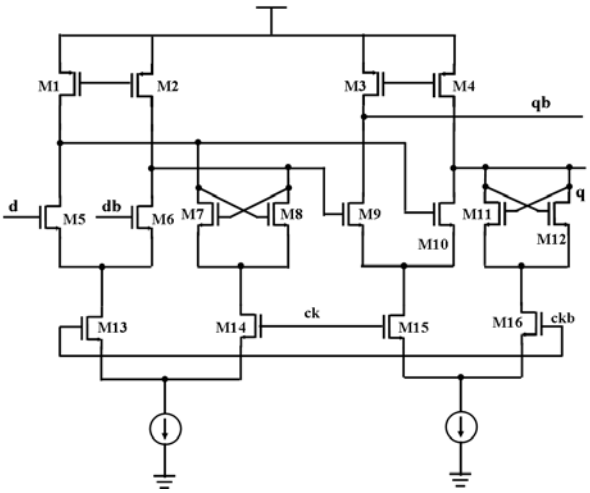

Figure 8. CML type Flip-Flop.

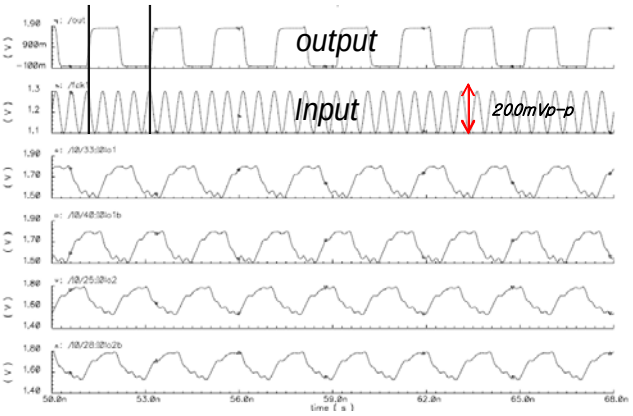

Figure 9. Simulation result of divider by 4/5.

Figure 9 shows the simulation result of divider by 4/5 circuits based on the CML type Flip-Flop.

3. EXPERIMENTAL RESULTS

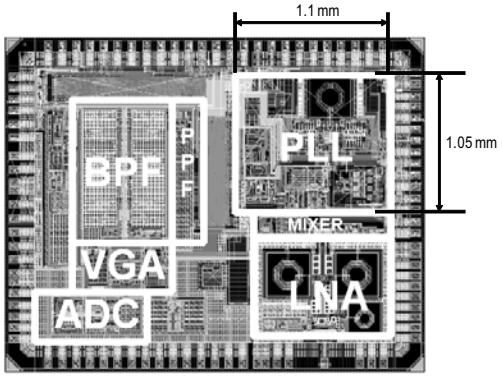

Figure 10. Chip microphotograph.

Figure 10 shows the chip microphotograph, and the die area of the frequency synthesizer is 1.1 x 1.05 mm^2.

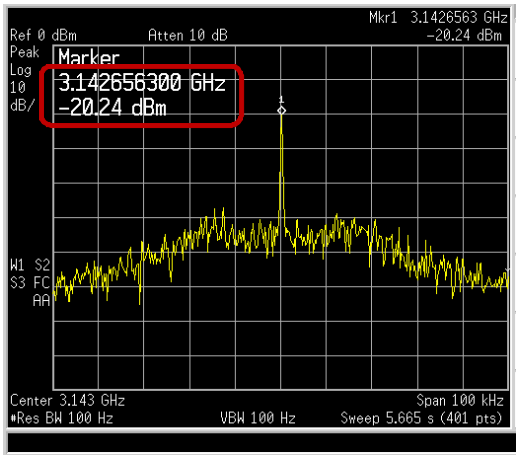

Figure 11. Measured spectrum of $2\times f_{LO}$ output.

Figure 11 shows the measured spectrum of the VCO output at 3.142GHz. Its power level is -20dBm at the VCO buffer output.

The phase noise of the VCO output at 3.142GHz is -120dBc/Hz at 1MHz offset as shown in Figure 12 and therefore the LO signal has -126dBc/Hz phase noise at 1MHz offset from the carrier.

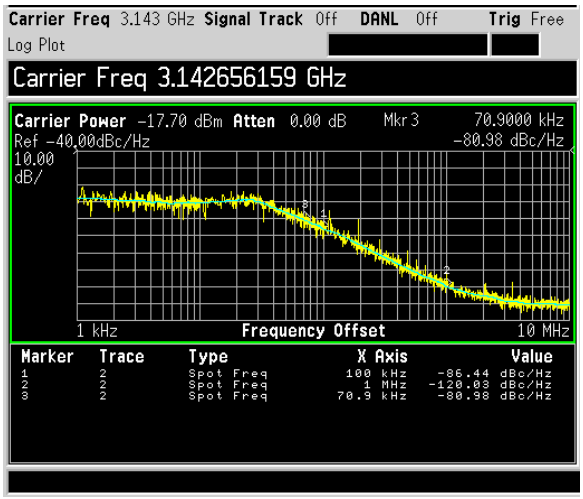

Figure 12. Measured phase noise of $2\times f_{LO}$ output.

Table I summarizes the performance of the GPS frequency synthesizer. The reference clock whose frequency is between 13MHz and 33MHz can be used for the designed fractional-N frequency synthesizer.

Table 1.
Performance summary of the GPS frequency synthesizer

Process	0.18μm CMOS
Active area	1.1 x 1.05 mm^2
Power	18mW @ 1.8V
Phase noise	-126dBc/Hz @ 1MHz
PLL reference frequency	13MHz ~ 33MHz

ACKNOWLEDGEMENT

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