A Shift Register for Gate Drivers Using P-Type LTPS TFTs

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Abstract: A shift register for gate driver is proposed using p-type LTPS TFTs. The proposed shift register is composed of three TFT and one capacitor employing 4 clock signals of 10V swing. Power consumption of the proposed scheme is 24.7% less than that of the previously reported shift register by refreshing the gate voltage of the output TFT with VDD.

1. Introduction

Gradually, the market for mobile application displays has been growing. To reduce the cost of the displays, it is important to reduce the size of the driving ICs. Driving ICs can be integrated with pixel array on a glass substrate by using the advantages of Low Temperature Polycrystalline Silicon (LTPS) technology. Therefore, this enables the creation of display systems of a more compact size. However, these display systems based on LTPS technology still need many external ICs.

These external ICs prevent the lowering of the cost of the display system because they take up a large portion of the overall system cost. Additionally, to reduce the process cost, p-type LTPS TFT circuits are preferred because a p-type LTPS TFT process can provide more cost benefits than a CMOS-type TFT process due to the reduced number of masks and processing steps [1]. Also, p-type LTPS TFTs are more stable to the hot carrier effect than n-type TFTs. Thus, p-type LTPS TFTs circuits are being in the spotlight compared with CMOS-type TFT circuits in the point of cost and stability.

Figure 1 shows a schematic diagram of previously reported shift register [2]. This circuit is a p-type shift register composed of four TFTs and one capacitor. However, this shift register has high power consumption because the output voltage of the shift register has a voltage drop by leakage current of output TFT, T3, through coupling between CLK_1 and gate of T3. In the proposed shift register, the voltage drop can be avoided by refreshing the gate voltage of the output TFT with VDD, and the power consumption can be reduced.

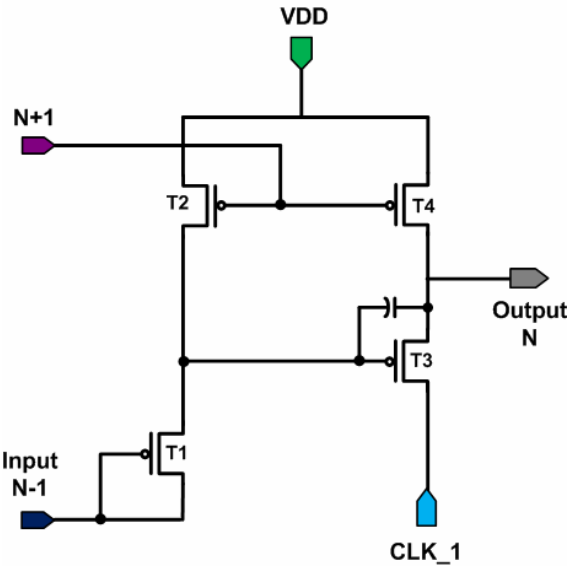

Figure. 1. The previously reported shift register.

2. Proposed Circuit

2. 1 The previously reported shift register

Figure 1 shows the schematic diagram of previously reported shift register for the gate driver. This shift register circuit has simple structure with four TFTs and a capacitor comparing to the gate driver with refeshing.

The T3 TFT pulls down the gate line of TFT-LCD. T2 and T4 TFT are connected with VDD which is reset voltage of T3 TFT and gate line of TFT-LCD. When the output signal of next shift register stage is generated, VDD supplies the gate line and T3 TFT gate for reset. For stable operation of the shift register during off period, clock coupling to the gate of T3 should be avoided. This circuit doesn't have a method to avoid clcok coupling. And, this increases the power consumption because the output voltage drops. In this paper, we proposed the shift register to solve this problem.

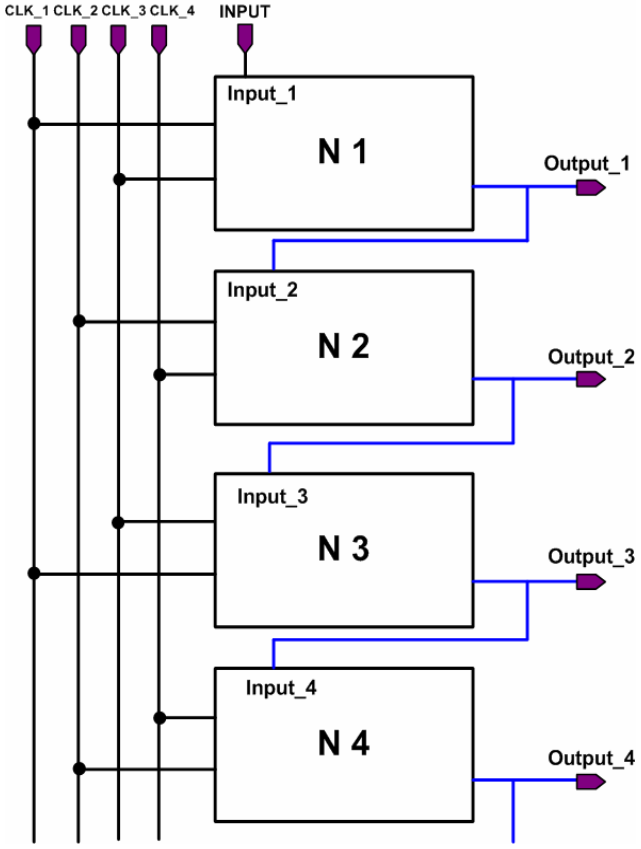

Figure. 2. The block diagrams of proposed shift register.

2. 2 The proposed shift register

Figure 2 shows a proposed shift register block diagram. This shift register consists of four clocks and one input pulse. Each stage operates in two clocks. In the first stage, the terminal Input_1 is conneted to a INPUT pulse signal. The N1 stage operates in CLK_1 and CLK_3. The Output_1 drives the gate line on panel and is connected to the terminal Input_2. Connecting relation in the next stage is similar to first stage, exception operating clocks. In the second stage, the N2 stage operates in CLK_2 and CLK_4. In the third stage, the N3 stage operates in CLK_3 and CLK_1. In the forth stage, the N4 stage operates in CLK_4 and CLK_2. Thus, we need four phases of clocks at least to implement the complete function of a gate driver.

Figure 3 shows the schematic diagram and timing diagram of the proposed shift register. This shift register consists of three TFTs and one capacitor.

In the first phase, T1 TFT turns on by input signal. Node A is charged by input voltage. The T3 TFT is on by input votage. However, the output is discharged, because CLK1 voltage is kept on "High." The T2 TFT is off beacese CLK3 voltage is kept on "High."

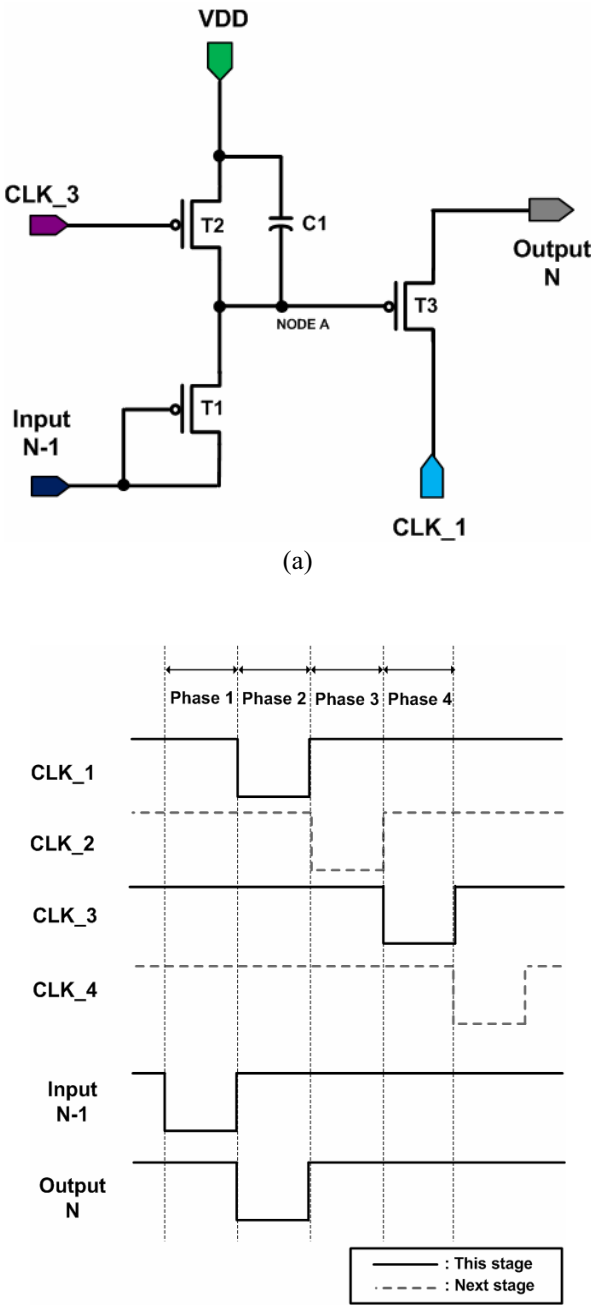

Figure. 3. The proposed unit shift register. (a) Schematic diagram and (b) Timing diagram.

In the second phase, CLK1 signal is "Low." Then voltage of node A is dropped by coupling of gate capacitor of T3 TFT. The T3 TFT gate voltage is lower than the input voltage because of the bootstrap effect. Finally, the output load is fully charged by the T3 TFT. The T2 TFT is still off beacese CLK3 voltage is kept on "High."

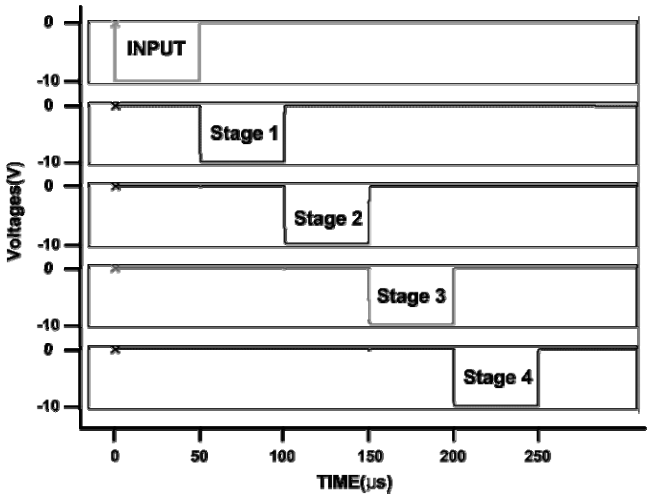

Figure. 4. The simulation result of proposed shift register using HSPICE.

In the third phase, CLK1 signal is "High." And, the T3 TFT is still on by the node A which is charged. Thus the output load is fully discharged by CLK1 signal. The T2 TFT is still off beacese CLK3 voltage is kept "High."

In the fourth phase, the T2 TFT is on by CLK3. The Node A is charged to VDD and then T3 TFT turns off. In order to sustain node A, there is a C1 capacitor between VDD and node A. The T2 TFT is on by CLK3 periodically. Therefore, the T3 TFT turns off periodically by T2 TFT. The periodical discharge method solves a clock coupling and output voltage drop problem.

Thus, we need four phases to implement the complete function of a proposed shift register.

3. Simulation Results

We simulated the proposed shift register using LTPS process. The input voltage is –10V. The clock swing voltage ranges from 0V to -10V. The resistance of gate line load is 3kΩ , and the capacitor of gate line load is 15pF. This is the gate line condition of 2.2" (QVGA) display.

Figure 4 shows the results of the proposed shift register. We can see that the input signal is shifting next stage.

Figure 5 shows the simulation output waveforms of previous shift register and proposed one. To operate stably and consume less power, the shift register should sustain the output wih 0V during one frame time. As shown in Figure 5(a), output voltage of previously reported shift register is coupled with clock. As a result, it drops by 1.03V during one frame time.

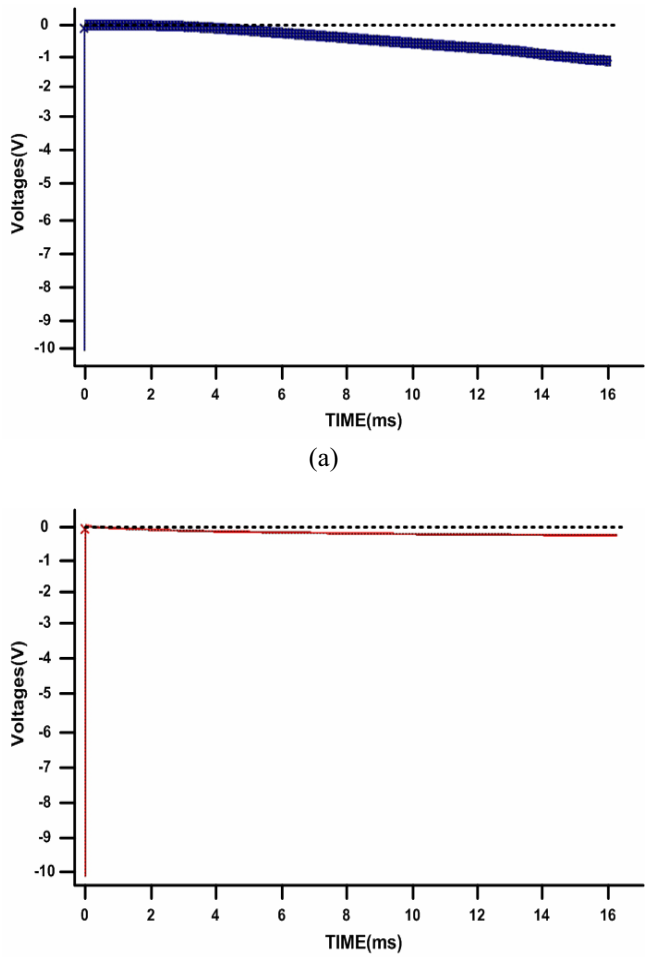

Figure. 5. The output waveforms of simulation result during one frame time. (a) Previous shift register and (b) Proposed shift register.

Table 1. The comparison of power consumption.

	Power consumption of one shift register during one frame time. (60Hz and 2.2" QVGA)
Previous Shift Register	0.11mW
Proposed Shift Register	0.083mW

As shown in Figure 5(b), the dropped voltage of our proposed scheme is 0.18V during the same period. As a simulation results, the proposed shift register can reduce the voltage drop.

And table 1 shows a comparison of the power consumption of the previous and our proposed shift register. The power consumption of the proposed shift register is 24.7% smaller than that of the previously reported one.

4. Conclusions

The proposed shift register consists of three p-type TFTs with one capacitor. The output voltage of the proposed shift register drops by 0.18V during one frame time. It reduces the output voltage drop by 0.85V in comparison to the previous reported one in the same period. Thus, we propose a p-type shift register with 24.7% less power consumption. By using this shift register, it is expected that a low-power and low-cost mobile display can be realized with LTPS technology.

References

[1] Y. –M. HA, "P-type Technology for Large Size Low Temperature Poly-Si TFT-LCDs," *SID Int'l Symposium Dig. Tech. Papers*, pp.1116 - 1119, 2000.

[2] H. Lebrum *et al*., "Design of integrated Drivers with Amorphous Silicon TFTs for Small Displays. Basic Concepts," *SID Int'l Symposium Dig. Tech. Papers*, pp. 950-953, 2005.