A Power-Efficient Voltage Up-Converting Circuit System

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Abstract: We developed a low-power voltage up-converter system that is composed of charge pump, level detector, and level shifter, which generates 1.0uA-10V from 2.5V VDD using 0.18um CMOS technology. The efficiency of the Dickson's charge pump was analysed with respect to the size of pumping capacitors and the number of pumping stages, and the optimum condition was chosen from the analysis results. The level detector senses VPP voltage in capacitive division way in order to eliminate the steady state VPP power dissipation through the resistive voltage divider. The power consumption in level shifters is reduced without sacrificing the switching speed by inserting a bootstrapped p-MOSFET between cross-coupled p-MOSFET and pull down n-MOSFET. Combing the three techniques the power consumption of voltage up-converting circuit system is saved by 28%.

1. Introduction

In last decades, the supply voltage has been constantly scaled in order to reduce the power consumption, as portable microelectronic devices have proliferated explosively. Some parts of the memory devices, however, still require much higher internal voltage(VPP) than the external supply voltage(VDD) for proper device operations. The efficiency of high voltage system has to be carefully managed in all areas including generation, maintenance, and consumption of elevated voltage sources as long as the power is concerned. The power-efficient voltage up-converter is, consequently, an important component in low power design of mobile hand sets if they have high voltage sub-blocks such as DRAM, flash memory, or RFID tag.

The voltage up-converting system consists of three function blocks: charge pump, level shifter, and level detector which are generator, consumer, and controller, respectively. This paper provides a thorough analysis of the three function blocks in terms of power efficiency. Dickson's charge pump is the most widely used voltage up-converter in many semiconductor devices including flash memories because it occupies small area when thin oxide capacitors are used [1]. The efficiency of the charge pump varies drastically with the number of pumping stage and the size of pumping capacitors. The level detector is a device to turn off the charge pump when VPP surpasses the preset level to save unnecessary pumping operations in the charge pump. It is inevitable that a small portion of VPP power is constantly leaking through a resistive voltage divider which is placed to monitor VPP level. Most of the VPP power is then consumed by level shifters and VPP drivers. The power consumption in a level shifter can be cut down only when we sacrifice the switching speed to some extent although a cascode level shifter is used [2]. We propose a voltage up-converter circuit system in which the power is decreased enough to be adopted in the memory IP of an RFID tag or other mobile appliances by making the three components power-efficient.

2. Voltage Up Converter

2. 1 Voltage Up Converter Circuit

The three components of a voltage up converter are connected as depicted in Figure 1. The pump supplies charge to VPP node to compensate the power consumed by level shifters and VPP drivers, and store the excess charge into the power capacitor as long as the level detector decides the VPP level is not sufficiently high. As the pump is turned off, VPP power is spplied from the power capacitor until the level detector concludes that VPP is low enough to resume pumping . The sensor in level detector has a hysteresis to avoid a bang-bang operation of the detector.

2. 2 Charge Pump

The Dickson's charge pump circuit shown in Figure 2 has been widely employed to generate elevated voltage source. The pump is made of pumping capacitors separated by diodes and the capacitors are alternatively powered by two non-overlapping clocks. The charges are pushed stage by stage from VDD side to the VPP side, resulting in higher DC voltage at the output port. The performance of Dickson's charge pump influences achievable VPP level and drivable Ipp current. The maximum VPP and Ipp are dependent on both the number of pumping stage and the size of pumping capacitors. A specified VPP level and Ipp
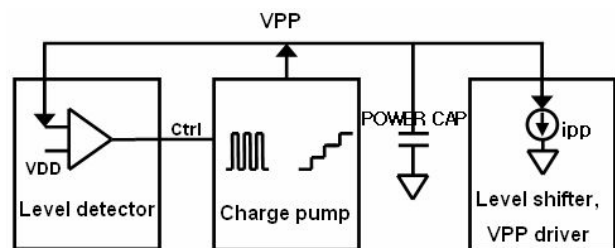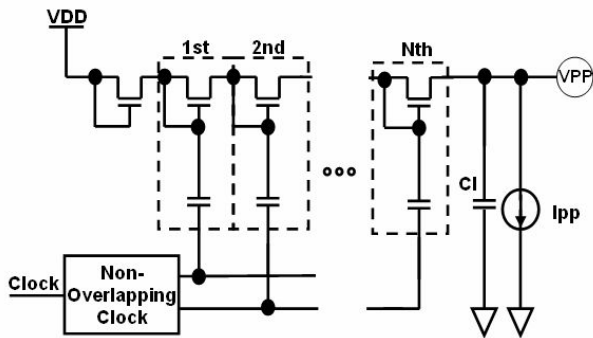

Figure 1. Voltage up converter system.

Figure 2. Dickson's charge pump

Table 1. Optimum number of stage and size of pumping capacitors, and the VDD current of charge pump for different VPP power.

Ipp	#Stage	Cp	Idd	Ipp/Idd
0.01uA	8	0.9pF	1.34uA	0.007
0.1uA	10	0.5pF	2.38uA	0.042
1.0uA	10	9pF	13.54uA	0.074
10uA	18	20pF	193.42uA	0.052

can be satisfied by different combinations of stage count and capacitor size, although each combination shows different power efficiency. The efficiency of a charge pump is defined as the ratio of the total Ipp current to the input current, Idd. We performed extensive HSPICE simulations with 1MHz clock to find out optimum power efficiency for several power requirements. One can notice that the VPP level is lowered as the total Ipp consumption is increased for a given charge pump. Both VPP and Ipp are increased with more stage count and bigger capacitor size as shown in Figure 3. The power efficiency shows a maximum when Ipp is drawn with proper number of pumping stage and appropriate size of pumping capacitors. At more stage with
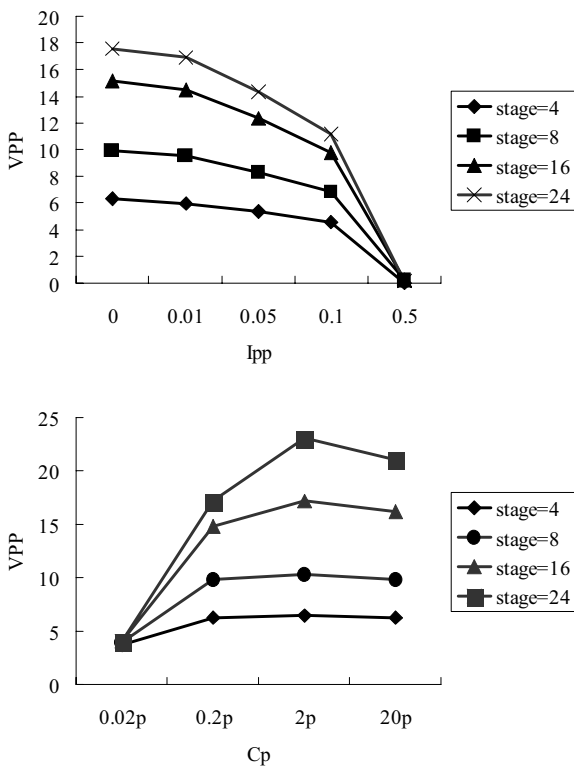
smaller capacitors waste unnecessary power due to imperfect charge transfer between stages. On the other hand, less stages with larger capacitors, the charge transfer is not completed during a clock cycle.

The optimum stage count and capacitor size is summarized in Table 1 for Ipp requirement of 0.01, 0.1, 1.0, and 10.0uA of Ipp, when 2.5V is pumped to 10V. As the current requirement increases, the optimum number of stages and the optimum size of pumping capacitor increase, but the power efficiency has a maximum at intermediate Ipp current.

2. 3 Level Shifter

The level shifter transforms the VDD output to VPP one. The conventional level shifter circuit uses cross-coupled p-MOSFET(PMOS) and pull down n-MOSFET(NMOS) as shown in Figure 4(a)[4]. Since the NMOS is sized so strong that the state of PMOS half latch is easily flipped by gate bias on NMOS. The pull up speed is, however, dependent on the size of the PMOS. If the PMOS is oversized for improved pull up speed, the PMOS and NMOS are turned on simultaneously during the pull down cycle to burn short circuit current from VPP to ground[3]. It is painful because the VPP current can be compensated by charge pumping with poor efficiency. To make the matter worse, short circuit current delays pull down switching. Now, we have to trade off between the power dissipation and speed of the conventional level shifter. The PMOS size is compromised at which pull up and pull down speed is balanced.

If the short circuit current is effectively blocked, a large PMOS can be used for fast switching in both directions. The short circuit current in the proposed level shifter circuit is successfully blocked by inserting PMOS between the cross-coupled PMOS and pull down NMOS as shown in Figure 4(b). The gate bias of the additional PMOS is controlled by bootstrapping. It is (VDD – Vth) during pull up cycle, and (2VDD – Vth) for pull down cycle. For VPP higher than twice VDD, the short circuit current is not completely eliminated, but significantly reduced. When VPP is not much different from VDD, the pull up speed can be degraded. The suggested level shifter is expected to perform best when VPP is 1.5~3.0 times VDD.
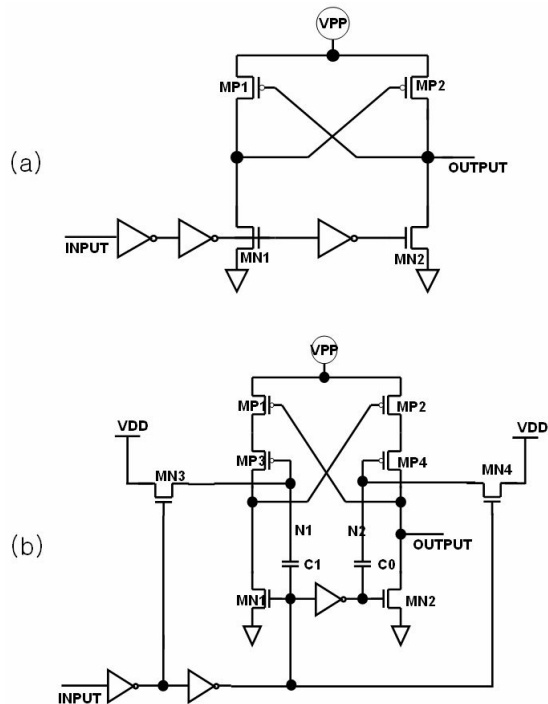

Figure 3. characteristics of a charge pump.

Figure 4. (a)Conventional and (b)power-efficient level shifters

Figure 5. Level detectors using (a)resistive and (b)capacitive division.

2. 4 VPP Level Detector

The VPP level detector is a controller for the voltage up-converting system. In general the size of the charge pump is designed to cover the maximum peak power dissipation of the chip. It is oversized when compared to the average power consumption. The VPP level goes higher than the desired level when we keep the charge pump running all the time. The VPP level detector is placed to turn off the charge pump when the VPP level reaches the preset voltage. Figure 5(a) shows a typical VPP level detector. Instant VPP level is sampled using a resistive divider. When VPP drops below 'Vref*(R1+R2)/R2' the enable signal (EN) is asserted to turn on the charge pump[5]. The resistive voltage divider burns constant VPP power proportional to the total resistance. If a very large resistor is used to save power dissipation, the response of the VPP regulator would be significantly delayed. The amplifier in the figure is a series combination of differential amplifier and Schmidt trigger. The Schmidt trigger has a thin hysteresis for which the bang-bang operation of the detector is prevented.

The proposed VPP detector circuit is using capacitors instead of resistors as a sampling means. Capacitive division level detector is operating as follows. In phase of precharge, the switches are connected as shown in Figure 5(b). The two inputs of differential amplifiers are precharged to Vref level. At evaluation state, the switches toggle to other state. Charge of VDD*C2 is pushed to lower branch of amplifier, and (VPP–VDD)*C1 is to upper branch. Those charges have to be equivalent if the input capacitance of differential amplifier is negligibly small when compared to C1 or C2. The resultant VPP is
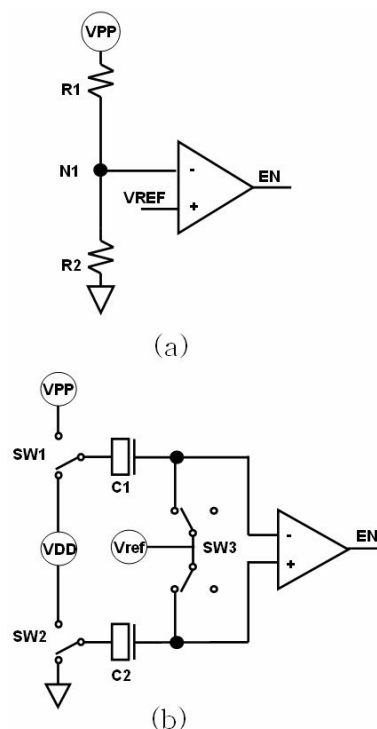
$[(C_1+C_2)/C_2]$*VDD. The important point in designing capacitive divider level detector is how to make the two inputs of differential amplifier floating. If there is any source of leakage current to/from the input nodes, the detector has to repeat precharging and evaluation to compensate the leakage. The dynamic power consumption is rooted out if SW3 is made of another capacitor through which coupling charge is used in precharging.

3. Simulation Results

The overall performance of a voltage up converting circuit system is evaluated by HSPICE simulation. The system is designed to supply 1.0uA-10V using 1MHz 2.5V input clock. The up-converter is targeted for 0.18um CMOS technology. The charge pump is extensively simulated to find best power efficiency in terms of the number of pumping stage and the size of pumping capacitors for given power requirement. Table 1 shows the optimum stage count and capacitor size at 0.01, 0.1, 1.0, and 10uA of Ipp.

Figure 6 shows simulation results of conventional and proposed level shifters. Due to effective blocking of short circuit current by bootstrapped PMOS peak current during pull down cycle is significantly reduced. For pull up transition, power consumption is decreased by quick transition although the peak current is hardly reduced. The VPP power dissipation and switching speed is compared in Table 2 for conventional and proposed level shifters. The
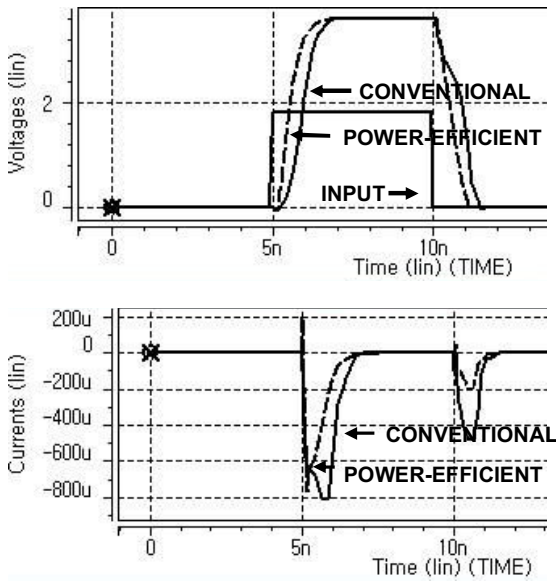
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Figure 6. Simulation results of conventional and power-efficient level shifter.

proposed level shifter spends less power by 69% when compared at comparable speed. The new level shifter reveals about one third of power delay product. To deliver 1.8V logic signal to 10V VPP domain, we built a two stage level shifter. VPP/VDD ratio in each step is allocated to be about 2.3. Figure 7 shows the simulated functional behavior of level detectors. When the charge pump output voltage reaches VPP+ΔV, VPP starts decline as the charge pump is turned off. The overall power consumption for the proposed voltage up-converting system is 72% of the conventional configuration.

4. Conclusion

Dickson's charge pump has been thoroughly analyzed in terms of stage counts and corresponding capacitor sizes to find configuration of best power efficiency at various power requirements. As required Ipp current increases,

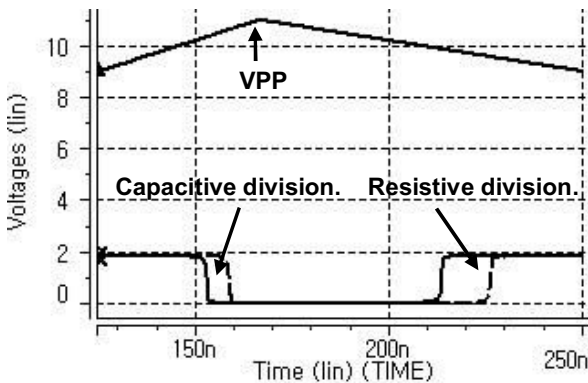Figure 7. Simulation results of level detector.

Table 2. Performance comparison of conventional and improved level shifters at 3.6V

	conventional	proposed
I-avg@100MHz	114.6uA	57uA
Delay	0.97ns	0.6ns
Power	412.56uW	205.2uW
Power delay product	400.18fJ	123.12fJ

optimum stage count and capacitor size increase, but power efficiency has maximum at intermediate power requirement. A level shifter equipped with a PMOS current blocking transistor between cross-coupled PMOS and pull-down NMOS saves power dissipation by 69%. Capacitive VPP sampling at level detector also contributes power reduction by eliminating standby VPP current. Combining the three power-efficient key components, the proposed voltage up converter can reduce power consumption by 28% for 1.0uA-10V generation from 2.5V clock using 0.18um CMOS technology.

Acknowledgment

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