A neuron MOS current mirror with a transimpedance amplifier

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Abstract: In this paper, we proposed a neuron MOS current mirror with a transimpedance amplifier. The conventional circuit is composed of a voltage amplifier and resistances. However, the resistance voltage drop makes operating range narrow. The proposed circuit is composed of the transimpedance amplifier. And the proposed circuit will be high current copy accuracy and wide operating range. The neuron MOS current mirrors are designed by using device parameter of the standard CMOS 1.2μm process. The performance of the proposed circuit is evaluated by HSPICE simulation. Simulation results show that the proposed circuit has better current copy accuracy without the resistances, and low voltage operation.

1. Introduction

Recently, integrated circuits to consolidate digital circuits and analog circuits prevail. Performance of the digital circuit advances with miniaturization of the process in the CMOS integrated circuit. And the digital circuit is low power consumption. Because a supply voltage is shifting to lower voltage. However, miniaturization of the process increases channel length modulation effect. And the lowering supply voltage narrows operating range of the circuit. A current mirror is a very important circuit for analog integrated circuits. The current mirror is circuit that copies current which is used as a power supply circuit and an active load. The channel length modulation effect results in deterioration of current copy accuracy. We solved this problem by the current mirror with neuron MOSFETs[1], [2](neuron MOS current mirror[3], [4]). The conventional circuit is constructed from a voltage amplifier and resistances. Current copy accuracy of the conventional circuit is improved by high gain of the voltage amplifier and high resistances. But the high resistances make operating range narrow. In this paper, we proposed the neuron MOS current mirror with a transimpedance amplifier. The proposed circuit improves current copy accuracy without resistances. And operating range of the proposed circuit is wider than the conventional circuit.

2. Neuron MOSFET

A basic structure of the neuron MOSFET is illustrated in Fig.1. It is an N-channel MOSFET having a gate electrode that is electrically floating. N input gates are capacitively coupled to the floating-gate. The neuron MOSFET can be manufactured in a standard CMOS process. Property of the neuron MOSFET in the standard CMOS process is reported. And the neuron MOSFET is influenced by initial charge[5]. The terminal voltages and capacitance

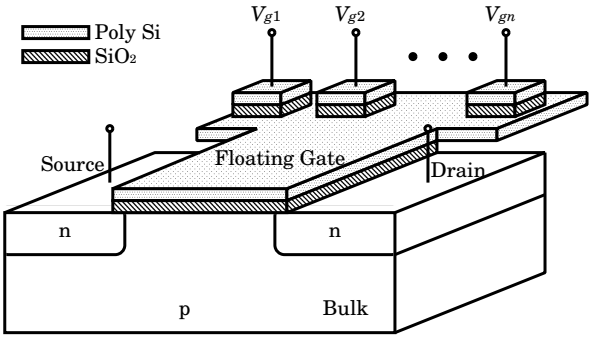


Figure 1. Neuron MOSFET structure.

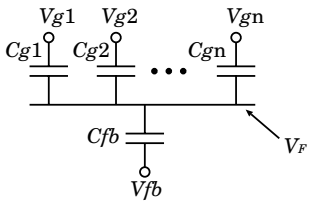


Figure 2. Relationship among terminal voltages and capacitance coupling coefficients.

coupling coefficients are defined in Fig.2, where V_F is the floating-gate potential, $V_{g1}, V_{g2}, \cdots, V_{gn}$ are the input signal voltages, $C_{g1}, C_{g2}, \cdots, C_{gn}$ are the capacitive coupling coefficients between the floating-gate and each of the input gates, C_{fb} is the capacitive coupling coefficient between the floating-gate and a bulk. The floating-gate potential V_F is calculated as

$$V_F = \frac{C_{g1}V_{g1} + C_{g2}V_{g2} + \cdots + C_{gn}V_{gn}}{C_{TOT}} \qquad (1)$$

where

$$C_{TOT} = \sum_{i=0}^{n} C_{gi} \qquad (2)$$

when

$$\frac{C_{g1}V_{g1} + C_{g2}V_{g2} + \cdots + C_{gn}V_{gn}}{C_{TOT}} > V_{TH} \qquad (3)$$

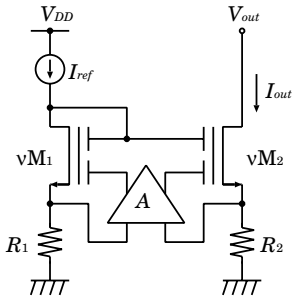


Figure 3. Conventional Circuit.

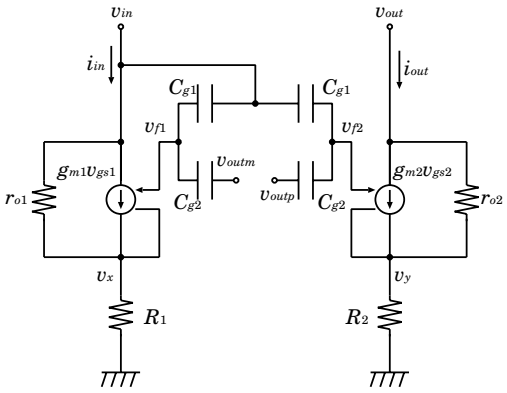


Figure 4. Small-signal equivalent circuit of the conventional circuit.

the neuron MOSFET operates. A drain current of the neuron MOSFET is given by

$$I_{DS} = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{FS} - V_{TH}\right)^2 = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(\frac{\sum_{i=1}^{n} C_{gi}V_{gi}}{C_{TOT}} - V_S - V_{TH}\right)^2 \quad (4)$$

where μ is a carrier mobility, C_{ox} is an oxide capacitance per area, W and L are a channel width and length, V_{FS} is the floating-gate voltage of the neuron MOSFET seen from a source voltage.

3. Output Resistance

The higher the output resistance, the higher the current copy accuracy of the current mirror. In this section, the output resistance of the conventional circuit and the proposed circuit is compared.

3.1 Conventional Circuit

The neuron MOS current mirror with the voltage amplifier is shown in Fig.3. R_1 and R_2 in Fig.3 convert the currents into the voltages. The voltage amplifier amplifies difference of these voltages. And it returns to the second gate of $\nu\mathrm{M_i}$. This will be high current copy accuracy.

Fig.4 is a small-signal equivalent circuit of the conventional circuit, where r_{o1} and r_{o2} are drain resistances. An input current and an output current in Fig.4 are given by

$$i_{in} = g_{m1}(v_{f1} - v_x) + \frac{v_{in} - v_x}{r_{o1}} \quad (5)$$

$$i_{out} = g_{m2}(v_{f2} - v_y) + \frac{v_{out} - v_y}{r_{o2}} \quad (6)$$

v_{f1} and v_{f2} are floating-gate voltages, so from equation (1), v_{f1} and v_{f2} are given by

$$v_{f1} = \frac{C_{g1}v_{in} + C_{g2}v_{outm}}{C_{g1} + C_{g2} + C_{fb}} \quad (7)$$

$$v_{f2} = \frac{C_{g1}v_{in} + C_{g2}v_{outp}}{C_{g1} + C_{g2} + C_{fb}} \quad (8)$$

where v_{outm} and v_{outp} are the output voltages of the voltage amplifier. v_x and v_y are resistance voltage drops, so v_x and v_y are given by

$$v_x = i_{in}R_1 \quad (9)$$

$$v_y = i_{out}R_2 \quad (10)$$

From equation (5)-(10), output resistance of the conventional circuit is given by

$$R_{out} = \left.\frac{v_{out}}{i_{out}}\right|_{i_{in}=0} \approx Ag_{m2}r_{o2}R_2\frac{C_{g2}}{C_{g1} + C_{g2} + C_{fb}} \quad (11)$$

where A is the gain of the voltage amplifier. The output resistance of the conventional circuit is high resistance when A and R_2 are higher.

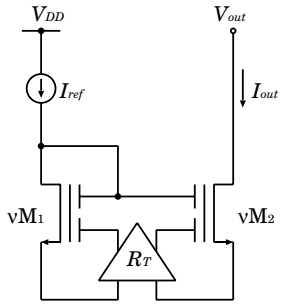


Figure 5. Proposed Circuit.

3.2 Proposed Circuit

The neuron MOS current mirror with the transimpedance amplifier is shown in Fig.5, where R_T is transimpedance of the transimpedance amplifier. The proposed circuit improves current copy accuracy without R_1 and R_2. The transimpedance amplifier amplifies a difference of I_{ref} and I_{out}. And it returns to the second gate of $\nu\mathrm{M_i}$. This will be high current copy accuracy.

Fig.6 shows the small-signal equivalent circuit of the proposed circuit. v_x and v_y in Fig.6 are given by

$$v_x = i_{in}R_{in} \quad (12)$$

$$v_y = i_{out}R_{in} \quad (13)$$

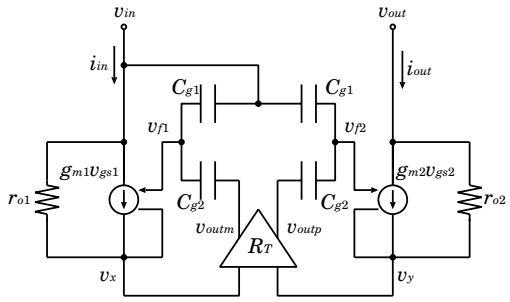
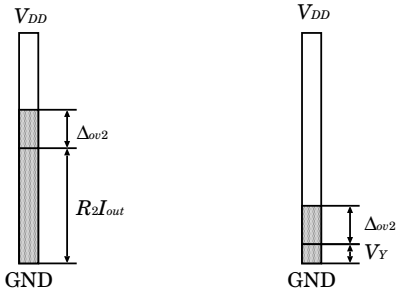


Figure 6. Small-signal equivalent circuit of the proposed circuit.



(a) Conventional. (b) Proposed.

Figure 7. Operating Range.

where R_{in} is input resistance of the transimpedance amplifier. From equation (5)-(10), and (12), (13), and with the condition that is $R_T \gg R_{in}$, we can obtain the output resistance as

$$R_{out} \approx g_{m2} r_{o2} R_T \frac{C_{g2}}{C_{g1} + C_{g2} + C_{fb}} \tag{14}$$

The output resistance of the proposed circuit is high resistance when R_T is higher. The output resistance of the proposed circuit is higher than the output resistance of the conventional circuit when

$$R_T \geq AR_2 \tag{15}$$

4. Opareting Range

4.1 Conventional Circuit

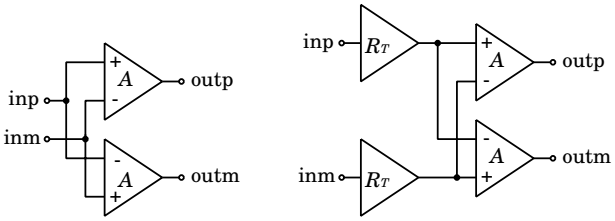
The output voltage for $\nu\mathrm{M}_2$ to operate in the saturation region is sum of an over drive voltage of $\nu\mathrm{M}_2$ and the resistance voltage drop. So operating range of the conventional circuit is given by

$$V_{out} \geq \Delta_{ov2} + I_{out} R_2 \tag{16}$$

where Δ_{ov2} is the over drive voltage of $\nu\mathrm{M}_2$. Operating range of the conventional circuit is shown in Fig.7(a). If R_2 is a low resistance, operating range is wide. However, the output resistance is the low resistance when R_2 is the low resistance.

Table 1. Parameter values of each elements in the neuron MOS current mirrors.

$\nu\mathrm{M}_{1,2}$	W=2.96[μm], L=1.48[μm]
I_{ref}	10[μA]
V_{DD}	3.0[V]



(a) Voltage Amplifier. (b) Transimpedance Amplifier.

Figure 8. Internal Circuit.

4.2 Proposed Circuit

The output range for $\nu\mathrm{M}_2$ of the proposed circuit to operate in the saturation region is sum of an overdrive voltage of $\nu\mathrm{M}_2$ and V_Y. So operating range is given by

$$V_{out} \geq \Delta_{ov2} + V_Y \tag{17}$$

Operating range of the proposed circuit is shown in Fig.7(b). If V_Y is low voltage, operating range is wide. And V_Y has no discernible impact on the output resistance. So the proposed circuit improves current copy accuracy with wide operating range.

5. Evaluation of Proposed Circuit

In this section, we compare the proposed circuit, the conventional circuit, and a low voltage cascode current mirror[6], [7]. These three current mirrors will be compared about the output resistance and operating range.

5.1 Parameter of the neuron MOS current mirros

Parameter of the neuron MOS current mirrors are shown in Table1. And internal circuits of the neuron MOS current mirrors are shown in Fig.8. A voltage amplifier of the conventional circuit is constructed from two voltage-controlled voltage sources. A transimpedance amplifier of the proposed circuit is constructed from two current-controlled voltage sources and two voltage-controlled voltage sources. A and R are 1000 and 30[kΩ] in the conventional circuit. $R_T \times A$ in the proposed circuit is 30[MΩ] to meet equation (15).

5.2 Low-Voltage Cascode Current Mirror

The low-voltage cascode current mirror is shown in Fig.9. The low-voltage cascode current mirror is commonly used. The output resistance of the low-voltage cascode current mirror is given by

$$R_{out} = g_{m2} r_{o2} r_{o4} \tag{18}$$

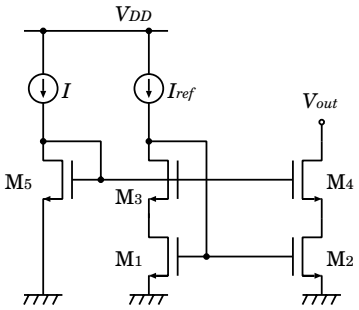


Figure 9. Low-voltage cascode current mirror.

Table 2. Design parameters of the low-voltage cascode current mirror.

$M_{1,2,3,4}$	W=2.96[μm], L=1.48[μm]
M_5	W=2.96[μm], L=5.92[μm]
I_{ref}, I	10[μA]
V_{DD}	3.0[V]

where r_{o1} and r_{o2} are the drain resistances of M_1 and M_2. And operating range of the low-voltage cascode current mirror is given by

$$V_{out} \geq \Delta_{ov2} + \Delta_{ov4} \tag{19}$$

where Δ_{ov1} and Δ_{ov2} are the over drive voltages of νM_1 and νM_2. Table 2 shows the design parameters of the low-voltage cascode current mirror.

5.3 Simulation Results

These three current mirrors are evaluated through HSPICE simulation with On-Semiconductor 1.2μm CMOS device parameters (LEVEL 28 models for HSPICE). A macro-model of the neuron MOSFET used the one of the T.Inoue[8].

Simulation results are shown in Fig.10 and Table 3. The neuron MOS current mirrors have better current copy accuracy than the low-voltage cascode current mirror. And the proposed circuit has wider operating range than the conventional circuit and the low-voltage cascode current mirror.

6. Conclusion

In this paper, a neuron MOS current mirror with a transimpedance amplifier has been proposed. A proposed circuit was composed of the transimpedance amplifier as internal amplifier. Then the proposed circuit improved current copy accuracy without resistances. Therefore the proposed circuit has been low voltage operation.

The proposed circuit was evaluated by the HSPICE simulation. The simulations showed that the proposed circuit

Table 3. The output resistances of the current mirrors.

	Fig.3	Fig.5	Fig.9
R_{out}	2.18[MΩ]	2.54[GΩ]	108[MΩ]

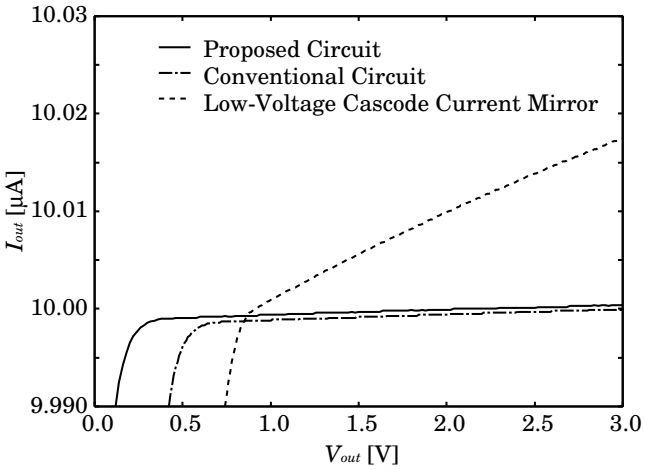


Figure 10. I_{out}-V_{out} characteristics.

operated in the low voltage ($V_{out} \geq 0.3$[V]), and an output resistance of the proposed circuit was high resistance ($R_{out} = 2.54$[GΩ]).

Acknowledgment

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