Low-power Standard Cell Memory using Silicon-on-Thin-BOX (SOTB) and Body-bias Control

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Abstract: In recent years, energy harvesting and sensor node have attracted a lot of attention. Therefore, a memory which can reduce power consumption and realize ultra-low voltage operation is required. However, it is especially difficult for the conventional SRAM to operate at ultra-low voltage. This paper describes a design of low-power Standard Cell Memory (SCM) using Silicon-on-Thin-BOX (SOTB). In particular, we present a novel layout sturucture for optimal body-bias control for SCM. Simulation results demonstrated that our SCM circuit can reduce leakage current by 53% and energy consumption in the active mode by 70-85% as compared to the SRAM circuit with the same circuit speed by body bias control. We also found that the SCM circuit can operate at the voltage lower than 0.2V under process variation by body bias control.

Keywords-- **ultra-low voltage operation, low-power, Standard Cell Memory, Silicon-on-Thin-BOX MOSFET, Body Bias**

1. INTRODUCTION

In recent years, energy harvesting and sensor node have attracted a lot of attention. For these applications, low-power consumption is strongly required. However, as device miniaturization of integrated circuits proceeds, leakage current and process variation problems become serious. In order to solve these problems, Silicon-on-Thin-BOX (SOTB) device which is one of the FDSOI devices has been proposed. SOTB can reduce the short channel effect and widely control Vth with the use of body biasing [1].

On the other hand, power consumption of a memory is increased in LSI. Although the conventional on-chip memories such as a cache or scratch-pad memory use SRAM which consists of six transistors, increase of its leakage power with device scaling and difficulty in lowering the operating voltage become a bottleneck at low-power oriented design. Operation of the SRAM is performed by detecting the current or voltage difference between the bit lines. It is difficult to operate at the ultra-low voltage because it is necessary to have operating margins under the consideration of variations. The supply voltage of SRAM within CPU operating at low-voltage is higher than core logic[2]. As a result, power consumption of CPU increases because leakeage power consumption of SRAM increases and lever-shifter is required. In order to solve these problems, a number of papers have already reported low voltage SRAMs which consist of six or more transistors[3]. Among them, there is also a study of SRAM using SOTB and body bias [4]. The former approach has the cost of larger area and higher active energy and operation at a higher supply voltage, whereas dedicated these soltions have a high design cost. Futhermore, SRAM cannot reduce leakage current easily in the active mode because SRAM is required to keep the static noise margin for read and write operations.

This motivated us to focus on the Standard Cell Memory (SCM) as a digital memory which is another option to supersede SRAM in CPU. SCM is made by the combination of standard cells. SCM has the feature that it enables us to design easily and it operates at low voltage. In [5] [6], the structure which uses a latch in a memory cell and NAND/NOR tree Multiplexers (MUX) in the read-out circuit was proposed. As a result, write and read energy of SCM is much smaller than SRAM[5]. However, the leakage current is also increased because area of SCM is larger than SRAM in general. In [7], custom latch to reduce leakage current has been proposed. This approach reduced leakage current and area by relaxing speed constraints. On the other hand, the authors did not focus on the structure and body bias. In this paper, SCM is made by the combination of standard cells in SOTB library. We propose an approach to apply body bias control for SCM using SOTB to reduce the leakage power consumption and active energy.

In this paper, we propose design and implementation methodology for SCM using SOTB and body bias, and demonstrate that SCM outperforms SRAM in power consumption and ultra-low voltage operation.

Section II compares SCM and SRAM under Zero body bias. Section III proposes body bias control for SCM and the layout of SCM based on the floorplan. Section IV shows the result of power consumption and minimum operating voltage by body bias control. Section V concludes the paper.

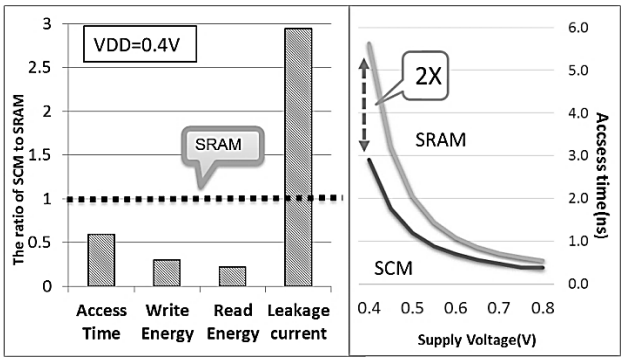
2. COMPARISONS BETWEEN SRAM AND STANDARD CELL MEMORY USING SOTB UNDER ZERO BODY BIAS

We clear the problems of SCM when we apply zero body bias(ZBB). We compared the performance of our designed SCM with that of the conventional SRAM in [4] by using HSPICE simulation. Figure 1 shows simulation results of access time, write energy, read energy and leakage current for ZBB. Write and read energy are composed of dynamic energy and leakage energy per operation. In simulation conditions, SCM is made by the combination of standard cells: Memory cells is Latch,

output selector is MUX and so on. Supply voltage is 0.4V and the memory size is 4Kbit (64word × 64bit). The write and read energy is measured when the 32bit data change from 0 to 1. Both of these memories were designed in commercial SOTB 65nm technology.

As shown in Fig.1(a), for ZBB, the access time, write energy and read energy of the proposed SCM are smaller than those for SRAM. Figure 1(b) shows the change in the access time by varying the supply voltage. Access time of the designed SCM is 2 times as fast as SRAM when supply voltage is 0.4V. The lower supply voltage, the larger this gap of access time. On the other hand, the leakage current has similarly increased because SCM has a larger area than the SRAM.

Figure 2 shows write, read energy and percentage of leakage in the entire energy in the active mode for each supply voltage. The minimum active energy is obtained at 0.35-0.4V in SCM. Furthermore, the lower supply voltage, the larger percentage of leakage. This result shows that it is important to reduce leakage current in the active mode when operating at low voltage.



(a)VDD=0.4 (b) VDD=0.4~0.8V

Fig. 1. Comparisons between the proposed SCM and SRAM in [4] for ZBB

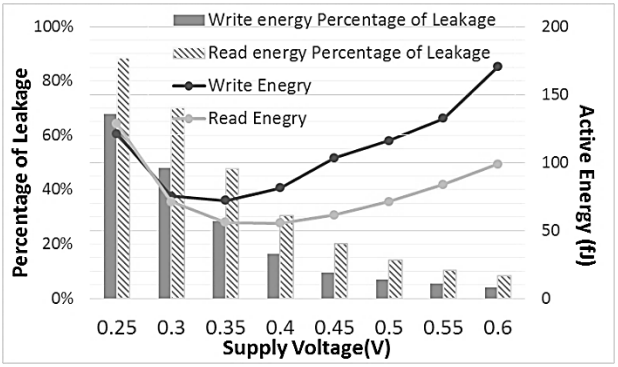


Fig. 2. Active energy and percentage of leakage when the 32bit data change from 0 to 1 in SCM

3. PROPOSED STANDARD CELL MEMORY USING SOTB AND BODY BIAS

3.1 Proposed body bias control for SCM

We propose a SCM using SOTB and body bias control for low-power consumption and ultra-low voltage operation. We mainly focus on the structure and read logic of SCM. In this paper, we mainly reduce leakage current of the latches without sacrificing performance because the dominant leakage contributors of SCM are the latches of memory cells.

We propose SCM floorplan and p-well/n-well structure for body bias control shown in Fig. 3. This proposed stems from the following:

1. Due to the constraint of triple-well constructure at SOTB, body bias control is performed at every two row to nMOS (nRBB) and the entire cells to pMOS (pRBB).

2. We study the balance of nRBB and pRBB voltages to each area, and obtain optimal body bias control from the viewpoint of energy efficiency (e.g., pRBB is nRBB+0.2-0.3V when supply voltage is 0.4V) .

3. We focus on the structure and read logic of SCM. Figure 4 shows a basic block diagram of SCM. Latch of SCM is on the non-critical path during read operation. On the other hand, MUX of SCM is on the critical path during read operation. Figure 5 shows the ratio of accsess time and leakage current by applying body bias separately. We clarified that the delay of latch is practically negligible during the read operation in Fig 5. As a result, it is possible to apply strong body bias to latch and remarkably reduce leakage current without increasing the delay. For this reason, nRBB can be applied to the latch and MUX separately as shown in Fig.3.

From the above, we propose body bias control for SCM. This approach applies body bias separately (nRBB of Latch, nRBB of MUX and pRBB of entire cells) and reduces leakage because we obtain optimal the balance of body bias control from the viewpoint of energy efficiency. We also reduce leakage without sacrificing performance of read operation because this body bias control is performed strongly at latch which is on non-critical path.

On the other hand, this body bias control degrades performance of write operation (e.g. write delay is 2 times as large as read delay). However, it is not always a problem. For example, cash memory requires the high performance of read time as compared with write time. It is possible to proceed to the next instruction because CPU uses a write buffer. Therfore, we are allowed to have some margin of write time as compared with the read time.

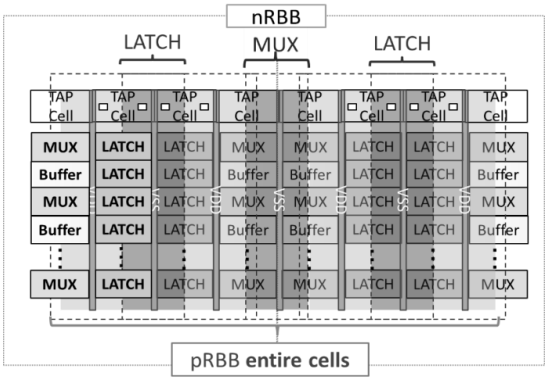


Fig. 3. Floorplan of proposed SCM

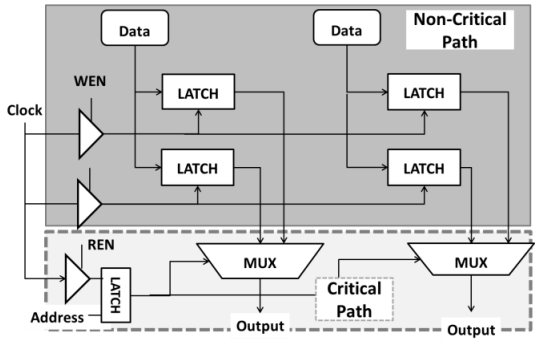


Fig. 4. A basic block diagram of SCM

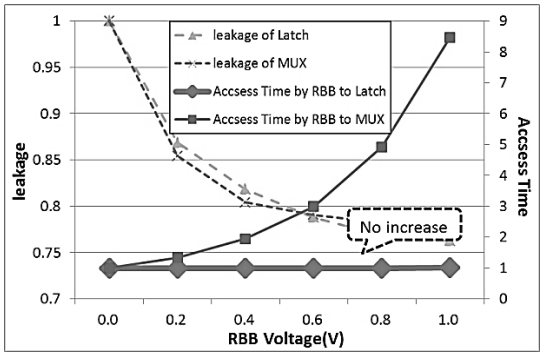


Fig. 5. The change in accsess time and leakage by RBB to Latch and MUX

3.2 Layout and floorplan

We designed the layout of SCM based on the floorplan shown in Fig.3 for performing the proposed body bias control. This layout is comprised of repetition of every two row of Latch or MUX. Figure 6 shows 4Kbit(64word×64bit) layout of SCM. It is easy to design because we designed the Macro of memory (8word×2bit) and the entire layout is designed by placing this Macro. However, circuit area of the designed SCM is 2.7 times as large as the conventional SRAM.

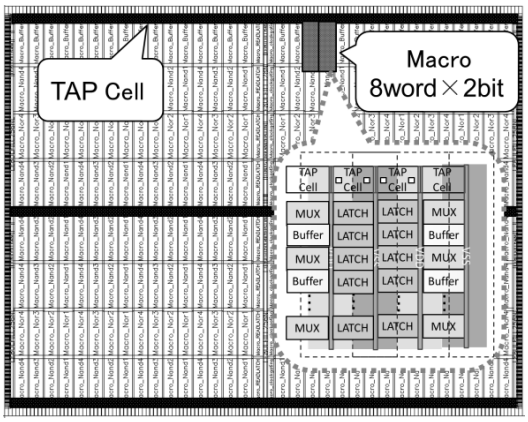


Fig. 6. 64word×64bit layout

4. RESULTS

We compared the performance of our proposed SCM with that of the conventional SRAM in [4] by using HSPICE simulation. Simulation condition is the same as that in Sec. II with the exception of applying body bias control.

4.1 Power consumption

Figure 7 shows comparisons between the proposed SCM and SCM under ZBB. In terms of the RBB voltage of SCM shown in Fig.7, nRBB of latch is 1.0V, nRBB of MUX is 0.2V and pRBB of the entire cells is 0.5V and the supply voltage is 0.4V. Access time of the proposed SCM is 2 times as large as SCM for ZBB. On the other hand, the write energy, read energy and leakage current of the proposed SCM are better than SCM for ZBB. Compared with SCM for ZBB, leakage current of the proposed SCM can be reduced by 86% by performing the proposed body bias control. Read energy of the proposed SCM also can be reduced by 25%. This body bias control for SCM can reduce not only leakage current but also active energy in the active mode in operating low voltage.

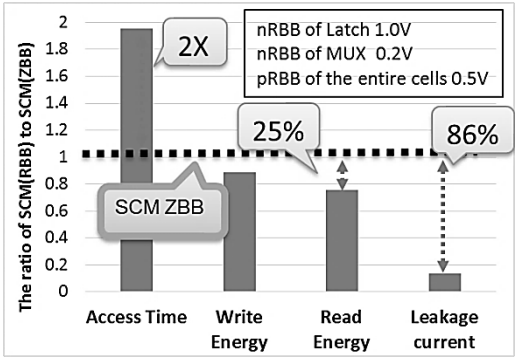


Fig. 7. Comparisons between the proposed SCM and SCM under ZBB

Next, we applied the body bias so as to make the access times of SRAM [4] and SCM be equal. In terms of the RBB voltage of SCM shown in Fig.8, nRBB of latch is 1.0V, nRBB of MUX is 0.2V and pRBB of the entire cells is 0.5V. Compared with SRAM with ZBB, leakage current of proposed SCM can be reduced by 53%. Moreover, write

and read energy can be reduced by 70-85%. This is because strong body bias can be applied to the latch and leakage current is remarkably reduced without increasing the delay.

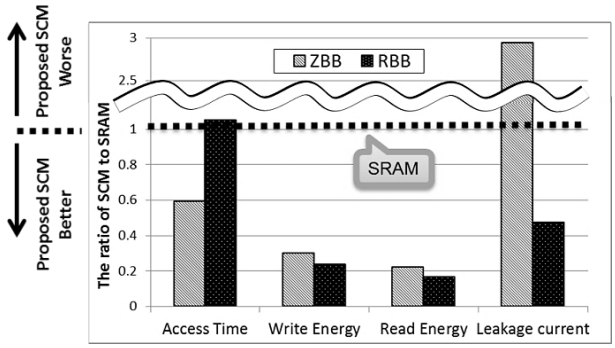


Fig. 8. Comparisons between the proposed SCM and SRAM in [4] for ZBB and RBB

4.2 Minimum operating voltage

We evaluated the minimum operating voltage of SCM under the temperature and process variations. We used similar simulations described in Sec. II with the exception of giving the temperature and process variations. We compared our proposed SCM with SRAM in [4]. In [4], the authors demonstrated that the minimum operating voltage is 0.37V by adaptive back bias.

Figure 9 shows simulation results of the minimum operating voltage. As a result, the worst minimum operating voltage of SCM is 0.27V for ZBB when the process variation is SS and the temperature is -30°C. This is because this condition gives the highest effective threshold voltage. Moreover, in high temperature, the worst minimum operating voltage of SCM is 0.22V for ZBB when the process variation is FS and temperature is 125°C. This is because this condition loses balance of nMOS and pMOS. These variations of minimum operating voltage are greatly affected by the variations of Vth. However, SCM using SOTB can widely control Vth with the use of body biasing. SCM operated at 0.12V at 25°C for FF condition for ZBB. It has been also demonstrated that SCM operated at 0.16V at -30°C and at 0.14V at 125°C by applying FBB and RBB, respectively. We found that this SCM circuit can operate at the voltage lower than 0.2V under process variation by body bias control.

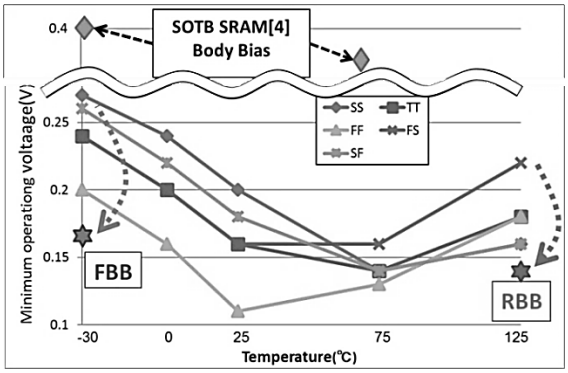


Fig. 9. Minimum operating voltage

5. CONCLUSIONS

In this paper, we presented the effectiveness of combining SCM and SOTB, and proposed layout structure for optimal body bias control for SCM. Additionally, we evaluated the power consumption and discussed the minimum operating voltage. Although there is a disadvantage that the SCM area is large, results demonstrated that our proposed approach enables us to design on-chip memories that achieve low-power consumption and ultra-low voltage operation without spending too much design time and effort.

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