

Design of 1 V Operating Fully Differential OTA Using NMOS Inverters

Atsushi Tanaka¹ and Hiroshi Tanimoto²

^{1,2}Department of Electrical and Electronic Engineering, Kitami Institute of Technology
165 Koen-cho, Kitami-shi 090-8507, Japan
E-mail : ¹mel07012@std.kitami-it.ac.jp, ²tanimoto@elec.kitami-it.ac.jp

Abstract: A 1 V operating fully differential OTA is presented. We designed a 1 V operating fully differential OTA using NMOS inverters in place of traditional differential pair. To obtain high voltage gain, a two stage configuration has been used in which the first stage has feedforward to cancel common-mode signal and the second stage has common-mode feedback. This OTA was fabricated by 0.18 μm CMOS technology. Measured dc gain is 40 dB and a unity gain frequency is 10 MHz. This OTA leads a solution to the low supply voltage issue in scaled CMOS analog circuits.

1. Introduction

The operation of analog circuits from low supply voltages becomes necessary due to down scaling of technologies. In the near future, the operation of analog circuits from 1 V supply voltage will be indispensable (Figure 1 [1]). However, it is difficult for traditional fully differential OTA using differential pair to operate from 1 V supply voltage. There is an idea using CMOS inverters in place of the differential pair to lower its operating voltage [2], [3], however, CMOS inverters require at least $2V_{th}$ so that the low supply voltage operation below 1 V may be difficult.

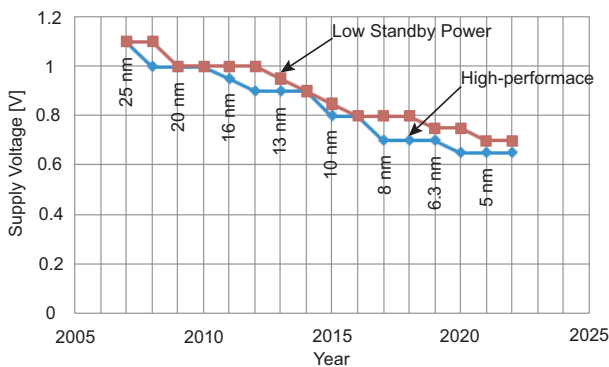


Figure 1. Supply voltage trend (ITRS road map)

On the other hand, it is possible for NMOS inverters to operate from lower supply voltages than CMOS inverters. A 0.9 V operating fully differential OTA using NMOS inverters have been reported [4]. However, the OTA cannot control its common-mode output voltages by itself, because it has only feedforward paths to cancel common-mode signals. On the other hand, the cascade connection of feedforward OTA and feedback OTA (F/F+F/B OTA) structure [3] can control its common-mode output voltages at the half of supply voltage by common-mode feedback. We designed and fabricated a 1 V operating fully differential OTA using NMOS inverters in

place of CMOS inverters in F/F+F/B OTA. Simulated and measured results are presented.

2. Issues in Low Supply Voltage Operation

A traditional fully differential OTA uses the differential pair. The differential pair is shown in Figure 2. This construction has more than three stacked MOSFETs between V_{DD} and GND, so that it is difficult for the differential pair to operate from supply voltages as low as 1 V. To overcome this situation, we must adopt circuits with less number of stacked transistors.

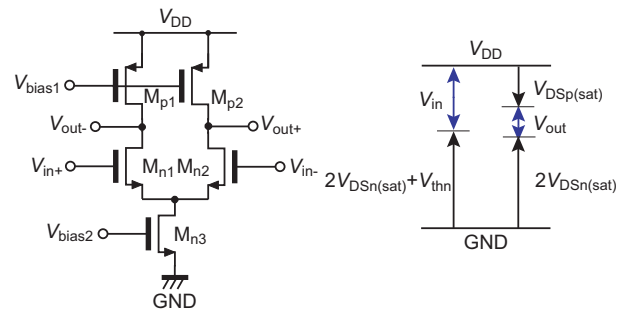


Figure 2. Differential pair

There has been some ideas using CMOS inverters in place of the differential pair to lower its operating voltage [2], [3]. The CMOS inverter is shown in Figure 3. This configuration has only two stacked MOSFETs between V_{DD} and GND. However, CMOS inverters still require at least $2V_{th}$ to operate so that the operation below 1 V may be difficult.

It is possible to lower the threshold voltage V_{th} by using additional process steps; however, it is not practical from the view point of increased production cost and leak currents in the digital circuit. Thus, we decided to adopt simple NMOS inverters, instead of CMOS inverters.

The NMOS inverter is shown in Figure 4. The use of a PMOS as a load current source makes it possible to determine the NMOS inverter's bias current independent of the V_{th} of NMOS. Therefore, it is possible for NMOS inverters to operate from lower supply voltages than CMOS inverters.

3. OTA Design

A circuit configuration of the F/F+F/B OTA is shown in Figure 5 [3]. This OTA consists a fully differential two-stage OTA, in order to obtain high gain. We could obtain only about 20~30 dB of voltage gain, if we used a single stage construction because of low output impedance of 0.18 μm CMOS process for the minimum gate length.

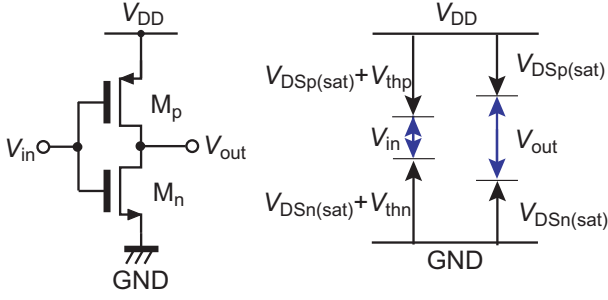


Figure 3. CMOS inverter (C-INV)

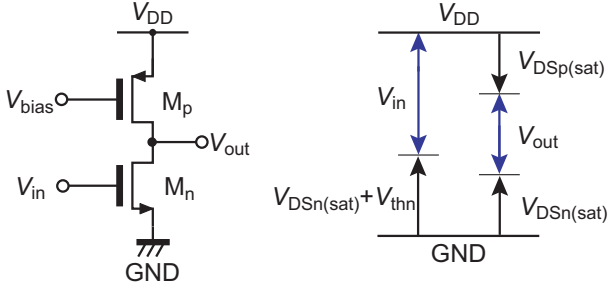


Figure 4. NMOS inverter (N-INV)

To suppress common-mode gain, this OTA has feedforward paths and feedback paths. The first stage has feedforward paths for common-mode cancellation, while the second stage has common-mode feedback paths to stabilize the output common-mode voltage. The input common-mode voltage is detected by averaging two inverted inputs, and only the inverted common-mode voltage is fedforward via two replica inverters (C-INV4, C-INV7) to the inverters in main signal paths (C-INV1, C-INV8). Likewise, the output common-mode voltage is also detected by averaging two inverted outputs, and only the inverted common-mode voltage is feedback via two replica inverters (C-INV12, C-INV15) to the inverters in main signal paths (C-INV9, C-INV16). Hence, the differential-mode signals are not fedforward or feedback because of the averaging. This is shown in Figure 6 (a).

Our main idea is to replace the CMOS inverters with NMOS inverters; however, simple replacements cause a problem. In the averaging stages, differential signal may not cancel out due to its class-A operation of the NMOS inverters. This is shown Figure 6 (b). This causes the differential-mode output to clip in its upper half portion, because some of the differential-mode component is feedback and lowers the differential-mode gain. This never occur if we use CMOS inverters.

To solve this problem, we decline to use the NMOS inverters to average in the F/F OTA and F/B OTA stages. The proposed OTA is shown in Figure 7.

First, we decline to use averaging action at the F/F OTA stage by disconnecting the outputs of N-INV3 and N-INV6. This permits signals to feedforward both common-mode and differential-mode; however, only the common-mode signals are canceled and the differential-mode signals aid due to the

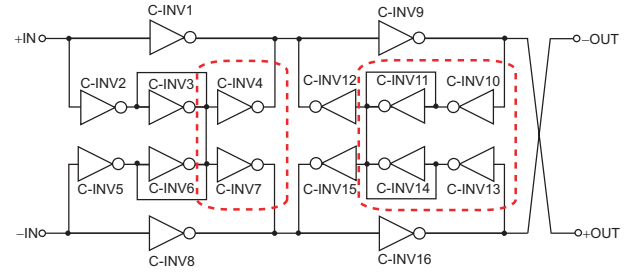


Figure 5. Configuration of F/F + F/B OTA

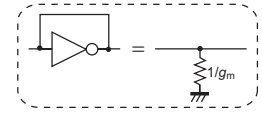
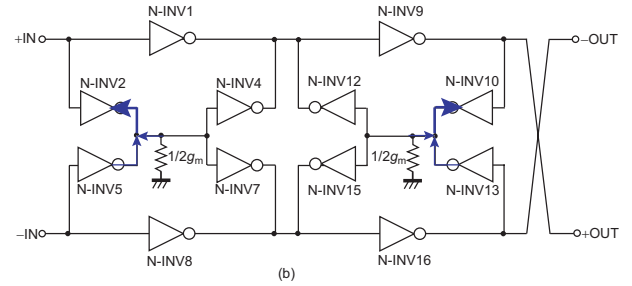
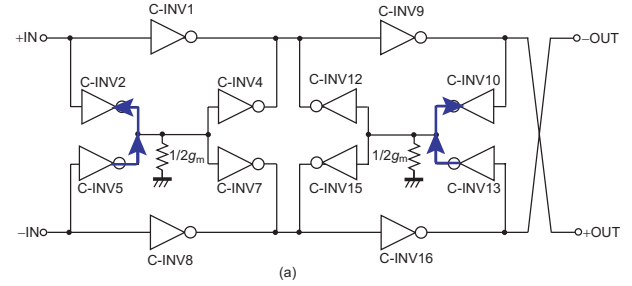


Figure 6. The flow of the differential signal of F/F+F/B OTA using CMOS inverters (a), and using NMOS inverters (b).

cross connection around the feedforward paths.

Second, in the F/B OTA stage, we adopted a resistive averaging circuit in front of the feedback circuit consisting of NMOS inverters (N-INV10~13). This eliminates the differential-mode signals input to the feedback circuit, and only the common-mode feedback remains. The resistance of the averaging circuit must be large in order to keep the voltage gain high. In this design $R = 220 \text{ k}\Omega$ is used, because the estimated output resistance of N-INV9(N-INV-14) is $22 \text{ k}\Omega$.

We assume a $0.18 \mu\text{m}$ CMOS process in the design. The gate length L of the NMOS inverters are $0.18 \mu\text{m}$ (minimum dimension) considering speed and power dissipation. Gate widths of the NMOS are designed to be $1.5 \mu\text{m}$, and those of PMOS are designed to be $6 \mu\text{m}$. The first stage inverters have all the same aspect ratio to keep common-mode cancellation high. In the second stage, main forward path inverters (N-INV9, N-INV14) have ten times the larger gate width than the first stage inverters, because they must provide larger output currents. Other inverters are the same dimension as that of

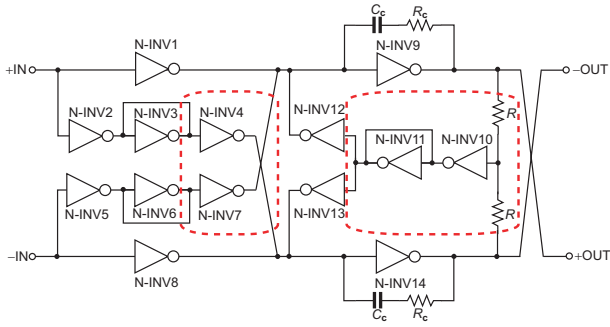


Figure 7. Proposed OTA

the first stage. Each unit inverter consumes about $5 \mu\text{A}$, and the output stage inverters consume about $50 \mu\text{A}$ from 1.0 V power supply. Total current consumption is about $170 \mu\text{A}$.

Because the proposed circuit is a two-stage amplifier, we introduced a conventional Miller compensation at the second stage as shown in Figure 7. The compensation capacitor C_c is 2 pF , and resistor R_c of $1 \text{ k}\Omega$ is put in series, in order to obtain phase margin of about 60 degrees. Simulated differential-mode gain is 44 dB , and the unity gain frequency is 13 MHz for no-load.

4. Simulated and Measured Results

The proposed OTA was designed and fabricated by using TSMC $0.18 \mu\text{m}$ 1P6M mixed signal CMOS technology. A micrograph of the fabricated OTA is shown in Figure 8. The size of the fabricated OTA is $315.5 \mu\text{m} \times 193.8 \mu\text{m}$. The large area of the right side is occupied by resistors of the averaging circuit ($2 \times 220 \text{ k}\Omega$).

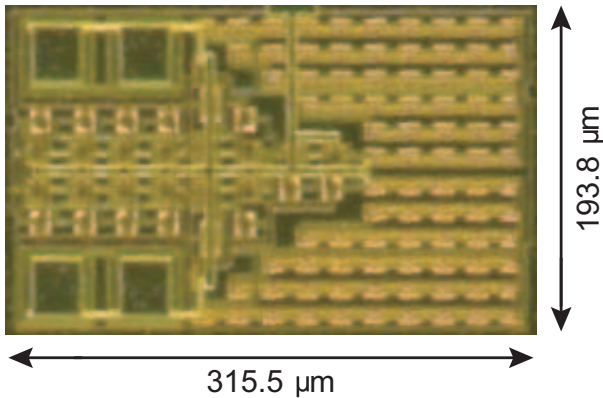


Figure 8. Chip micrograph of the proposed OTA

Figure 9 shows the simulated and measured frequency responses of the proposed OTA. The simulated differential-mode gain is 42 dB and the measured gain is 39 dB for a $100 \text{ k}\Omega$ load with a 13 pF capacitor in parallel. For common-mode, the simulated gain is -33 dB and the measured gain is -35 dB for the same condition.

These results indicate that the measured responses of the differential-mode are well matched with the designed responses.

The common-mode phase response could not be measured. Measurements for common-mode signal is difficult because the common-mode signal is very small due to a very large common-mode rejection ratio of the proposed OTA. However, because the measured common-mode gain is less than unity for all frequency range, a stability problem will not occur. Anyway, the measured results indicate its usefulness of the proposed circuit configuration operating at very low power supply voltage situations.

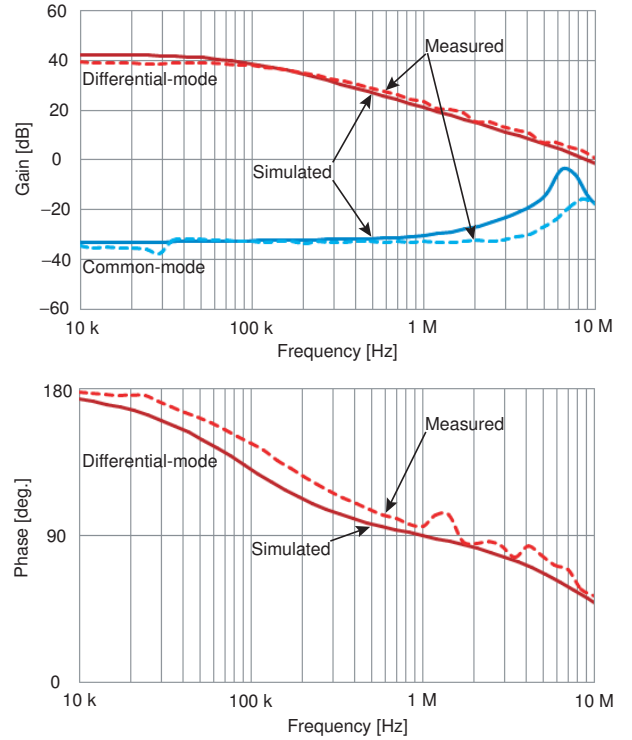


Figure 9. Bode plot of the proposed OTA

Figure 10 (a) shows measured output clipping levels to show the maximum output voltage swings of the two outputs. Each output voltage swings $880 \text{ mV}_{\text{P-P}}$ at 1 V power supply, as expected from the simulation result. Figure 10 (b) shows the maximum differential output voltage swing, which is $1.8 \text{ V}_{\text{P-P}}$ at 1 V power supply. It has been confirmed that the proposed OTA has a very large output swing capability even in a low power supply voltage.

The simulated and measured performances of the proposed OTA are summarized in Table 1. Unfortunately, its current consumption was not measured, because the power supply line is common to other circuits on the same chip.

5. Conclusion

We proposed an NMOS inverter based fully differential two-stage OTA, which can operate from 1 V power supply. The proposed OTA has been designed and fabricated in $0.18 \mu\text{m}$ CMOS process. The measured results confirm that the OTA can successfully operate from 1 V power supply with about 40 dB , unity gain bandwidth of about 10 MHz at $170 \mu\text{A}$ of

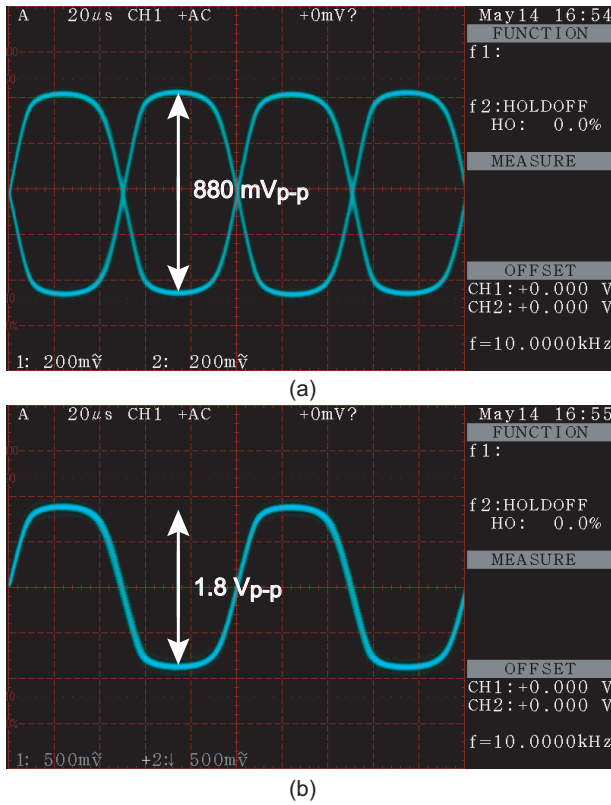


Figure 10. Measured output swing of the proposed OTA. Two single-end output voltages (a), and differential output voltage (b).

Table 1. Performance summary of the proposed OTA ($R_L=100\text{ k}\Omega$, $C_L=13\text{ pF}$)

Item	Simulated	Measured
Supply voltage	1.0 V	1.0 V
Current consumption	170 μA	–
Open-loop dc gain	42 dB	39 dB
Unity gain frequency	9 MHz	10 MHz
Phase margin	52 deg.	53 deg.
Output voltage swing	(28~974) mV	(50~ 930) mV
CMRR @10 kHz	75 dB	74 dB

current consumption. This OTA provides a solution to the low supply voltage issue in scaled CMOS analog circuits.

The differential-mode gain of the proposed OTA is lower compared with that of reference [3] in this design; however, we can improve its gain by using larger gate lengths. The proposed OTA can operate from lower supply voltage than the reference [3], and has better control over current consumption because it is based on class A inverters unlike class AB CMOS inverters in the reference [3]. The proposed OTA may be applied to integrated variable filters because its transconductance can be controlled by changing its operating current.

Acknowledgments

The authors thank Dr. H. Yanagisawa of Kitami Institute of Technology, for his support in preparing CAD tools. This work is partly supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

References

- [1] ITRS, "International Technology Roadmap for Semiconductors 2007 Edition Process Integration, Devices & Structures," http://www.itrs.net/Links/2007ITRS/2007_Chapters/2007_PIDS.pdf, April, 2008.
- [2] Bram Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE J. Solid-State Circuits*, Vol. 27, pp. 142–153, February, 1992.
- [3] Keishi Komoriyama, Eiichi Yoshida, Makoto Yashiki, Hiroshi Tanimoto, "A Very Wideband Fully Balanced Active RC Polyphase Filter Based on CMOS Inverters in 0.18 μm CMOS Technology," *Symposium on VLSI Circuits Dig. Tech. Pap.*, pp. 98–99, June, 2007.
- [4] Takeshi UENO, Tetsuro ITAKURA, "A 0.9 V 1.5 mW Continuous-Time $\Delta\Sigma$ Modulator for W-CDMA," *IEICE Trans. Fundamentals*, Vol.E88-A, No.2, pp 416–468, February, 2005.
- [5] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, New York, 2001.