Low-Voltage and High-CMRR Differential Amplifier Using FG-MOSFET's

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Abstract: In this paper, low-voltage and high-CMRR differential amplifier using two-input floating-gate MOSFET's is presented. The proposed differential amplifier is based on the bulk biasing technique proposed by Monsurrò. Monsurrò's amplifier, however, requires the low-boost circuits and twin-well process. In the proposed amplifier, these disadvantages are removed. The circuit is evaluated through Star-HSPICE with a set of device parameters of 0.35μm CMOS process. The simulations demonstrate a common-mode gain of -59.5dB and a differential gain of 16.2dB with $V_{DD} = 1.4$V. And the chip area is 131μm$\times$101μm from the mask layout design.

1. Introduction

Differential amplifiers are the one of the most important circuit element of analog integrated circuits including operational amplifier, OTA, active filters etc. In portable equipment systems operating at a single battery with low voltage is scaling down. The differential amplifiers are most susceptible to the reduction of the supply voltage [1]. In order to overcome this problem, tail current source is often removed from the differential amplifier. However, this method draws the deterioration of the CMRR, especially common-mode gain. Recently, the bulk biasing technique has been proposed by Monsurrò [2]. By using this technique, the differential amplifier can be operated at minimum supply voltage without deterioration of CMRR. This technique, however, is forced to used the twin-well process because the back-gates are used in this technique [2]. Furthermore, a low-boost circuit and clock generator for the low-boost circuit are necessary for the separation between the device and substrate [2].

In this paper, we propose the low-voltage and high-CMRR differential amplifier using multiple-input floating-gate MOSFET's (FG-MOSFET's). The proposed circuit can be realized by using standard CMOS process and requires no low-boost circuits. The proposed circuit is evaluated through Star-HSPICE with a set of device parameters of 0.35μm CMOS process. The detailed simulation results are reported in this paper.

2. Multiple-Input Floating-Gate MOSFET

Figure 1(a) shows the basic structure of the multiple-input FG-MOSFET proposed by Shibata and Ohmi as a functional MOSFET featuring a gate-level weighted sum and threshold operation [3]. It consists of an n-channel MOSFET with a floating gate (first poly layer) over the channel and, in some cases, extends to the field-oxide area. Multiple input gates are formed by the second poly layer over the floating gate. The capacitive coupling between the multiple input gates and the floating gate is shown in Fig. 1(b). C_0 shown in Figs. 1(a) and 1(b) is the capacitance between the floating gate and the substrate. Figure 1(c) is the symbolic representation of a multiple-input floating-gate MOSFET. Now, in the case of a k-input FG-MOSFET, capacitances between the multiple input gates and the floating gate are defined as $C_1, C_2, \cdots, C_k$, in order, from the drain side as shown in Fig. 1(c) (Fig. 1(c) is an example of the case of $k = 2$). Figure 1(d) shows an example of the physical layout of a FG-MOSFET.

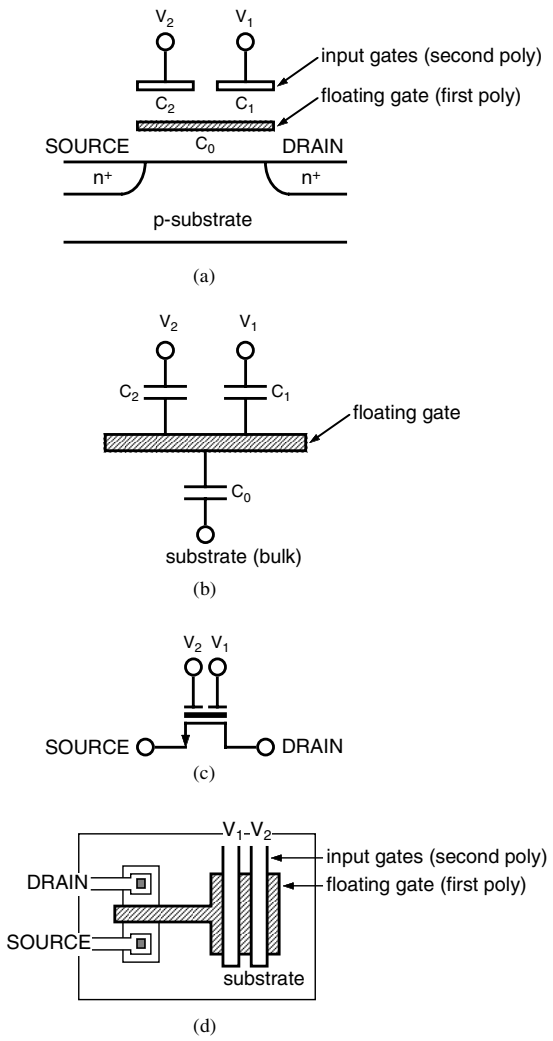

Figure 1. The multiple-input floating-gate MOSFET. (a) An illustration of the cross-sectional structure, (b) capacitive model, (c) symbolic representation and (d) physical layout.

When the floating-gate to source voltage (V_{fs}) is larger than the threshold voltage, as seen from the floating-gate

(V_T), the drain to source voltage (V_{ds}) is larger than $V_{fs} - V_T$ and the initial charge of the floating-gate equals 0, the FG-MOSFET operates in the saturation region. I_{ds} of the k-input FG-MOSFET under the saturation region is [3]

$$\begin{aligned} I_{ds} &= K\left\{\sum_{i=1}^{k}\frac{C_i}{C_0+\sum_{j=1}^{k}C_j}\left(\sum_{i=1}^{k}V_i - V_s\right) - V_T\right\}^2 \\ &= K\left\{\sum_{i=1}^{k}\omega_i\left(\sum_{i=1}^{k}V_i - V_s\right) - V_T\right\}^2 \end{aligned} \quad (1)$$

where $K(=\mu C_{OX}W/(2L)$ is the transconductance parameter, C_i is the capacitance between the floating-gate and i-th input-gate, C_0 is the oxide capacitance between the floating-gate and the substrate, V_s is the source voltage and V_T is the threshold voltage, as seen from the floating-gate. In Eq. (1), $W_i = \frac{C_i}{C_0+\sum_{j=1}^{k}C_j}$ is defined and referred to a capacitive weight. This device has a function of weight-sum operation as shown in (1). In the proposed circuit, this function is positively used. On the other hand, FG-MOSFET's have a issue of initial charge on the floating-gate in nature. This issue, however, can be overcome by using technique proposed in [4]. We also use the same technique shown in [4].

3. Proposed Differential Amplifier

Figure 2 shows the proposed differential amplifier. The circuit is divided two circuit blocks; one is the differential amplifier block (Block I) and the other is the bias voltage generator block (Block II). Figure 3 shows the detailed circuit schematic of Block II. From these figure, the number of active devices between V_{DD} and GND is two, which is as same as that of differential amplifier without the tail current source. In the proposed circuit, M_1, M_2, M_{1r}, and M_{2r} are the two-input FG-MOSFET's and are the same. M_{1r} and M_{2r} are used as replica devices of M_1 and M_2.

When common-mode signal is applied, drain currents of M_{1r} and M_{2r} in Block II are the same and its value is $I_B/2$. Then, error amplifier A detects the error voltage between the drain voltage of M_{1r} and M_{2r} (V_d) and V_{ref}. The voltage V_{BC}, which is the output voltage of the error amplifier, becomes input signal of the other terminal of FG-MOSFET's. The drain-to-source current of M_1 and M_2 is also $I_B/2$ because the floating-gate-to-source voltages (V_{fs}) of all FG-MOSFET's are the same value. Therefore, the bias current of Block I becomes $I_B/2$; the circuit is behaves the differential amplifier with a tail current source, although no tail current source in Block I.

Next, we consider the small variations around the bias point. If V_{in} is the common-mode signal ($v_{in,CM}$), from Eq. (1), v_{repl} and v_{bc} can be given by

$$v_{repl} = -A_{repl}\left(\omega_{in}v_{in,CM} + \omega_{bc}v_{bc}\right) \quad (2)$$

$$\begin{aligned} v_{bc} &= A_{amp}v_{repl} \\ &= -A_{amp}A_{repl}\left(\omega_{in}v_{in,CM} + \omega_{bc}v_{bc}\right) \end{aligned} \quad (3)$$

where A_{repl} is the voltage gain of M_{1r} and M_{2r} and is equal to $g_{mr}r_{outr}$ (in which g_{mr} and r_{outr} are the transconductance and output resistance of M_{1r} and M_{2r}, respectively)

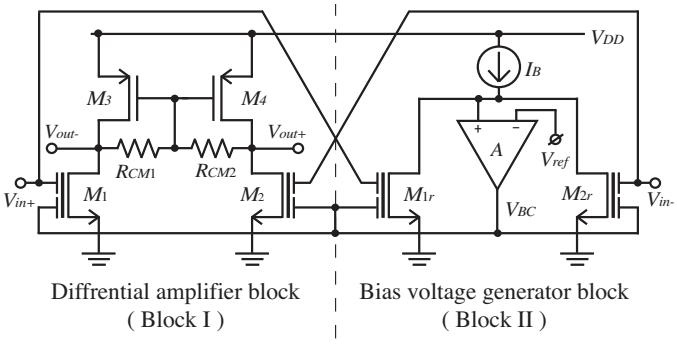

Figure 2. The proposed differential amplifier.

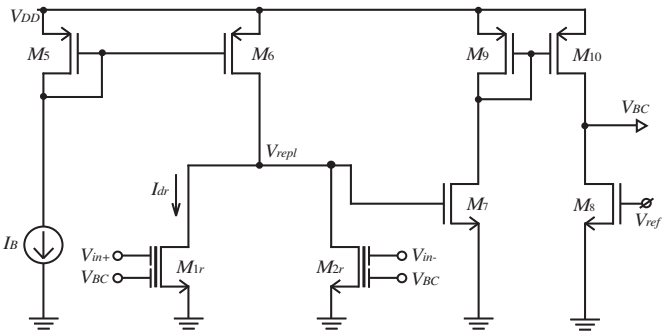

Figure 3. The circuit schematic of Block II.

and A_{amp} is the voltage gain of the non-inverting gain stage composed of M_7, M_8, M_9 and M_{10}, and ω_{in} and ω_{bc} are as follows.

$$\omega_{in} = \frac{C_{in}}{C_0 + C_{in} + C_{bc}} \quad (4)$$

$$\omega_{bc} = \frac{C_{bc}}{C_0 + C_{in} + C_{bc}} \quad (5)$$

Using Eq. (3), v_{bc} at steady state can be given by

$$v_{bc} = -\frac{A_{repl}A_{amp}\omega_{in}}{1 + A_{repl}A_{amp}\omega_{bc}}v_{in,CM} \quad (6)$$

Assigning Eq. (6) to (2), v_{repl} can be given by

$$v_{repl} = -\frac{A_{repl}\omega_{in}}{1 + A_{repl}A_{amp}\omega_{bc}}v_{in,CM} \quad (7)$$

Using Eq. (6), the bias current variation i_{dr} (the drain currents of M_1, M_2, M_{1r} and M_{2r}) can be given by

$$\begin{aligned} i_{dr} &= g_{mr}\left(\omega_{in}v_{in,CM} + \omega_{bc}v_{bc}\right) \\ &= \frac{g_{mr}\omega_{in}}{1 + A_{repl}A_{amp}\omega_{bc}}v_{in,CM} \end{aligned} \quad (8)$$

From Eq. (8), we can find that variation of i_{dr} with respect to $v_{in,CM}$ can be suppressed if $A_{repl}A_{amp}\omega_{bc}$ is enough large. Furthermore, v_{repl} with respect to $v_{in,CM}$ can be also suppressed from Eq. (7). As the results, the performance of the common-mode rejection can be improved.

Table 1. The designed element values in the proposed circuit.

Item		Value
V_{DD} [V]		1.4
V_{ref} [V]		0.6
R_{CM1}, R_{CM2} [kΩ]		200
C_{in} [pF]		0.74
C_{bc} [pF]		0.37
I_B [μA]		10
W/L [μm/μm]	M_1, M_2, M_{1r}, M_{2r}	5/1
	M_3, M_4	6/1
	M_5, M_6, M_7, M_8	4/1
	M_9, M_{10}	1/1

4. Simulation Results

The proposed differential amplifier is evaluated through Star-HSPICE simulation with 0.35μm double-poly three-metal CMOS process parameters. The designed values of devices are listed in Table 1. As shown in Table 1, the supply voltage (V_{DD}) is 1.4V.

Figure 4 shows the relation between the total bias currents (addition of the drain currents of M_1 and M_2) and $V_{in,CM}$. From this figure, $I_{d1} + I_{d2}$ is almost constant and its value is approximately 10μA in the range of 0.28V$< V_{in,CM} <$ 0.85V. The value is approximately equal to I_B as theory. And we confirmed that I_{d2} is as same as I_{d1}. Figure 5 shows the relation between V_{out1} (=V_{out2}) and $V_{in,CM}$. From this figure, output voltage is 0.6V, which is equal to V_{ref}, within a common-mode input range mentioned before. Figures 6 and 7 show the common-mode gain (A_c) and differential gain (A_d), respectively. From these figures, A_c is -59.5dB up to 10kHz and A_d is 16.2dB up to 10MHz. The current consumption of the proposed amplifier was 29.1μA. Figure 8 shows the start-up time interval, without any input signal. The steady-state current ($\simeq$ 10μA) is reached in about 600ns. A comparison of the main performance parameters of the differential amplifier with a tail current source, the differential amplifier without a tail current source and the proposed differential amplifier is summarized in Table 2. As shown in Table 2, we can confirm that A_c in the proposed circuit is drastically improved.

Figure 9 shows the results of the physical layout design. Especially, the parasitic capacitance between floating-gate and substrate is large value, and it degrades the amplifier gain. In order to reduce it, we used the metal wires to connect the gate of MOSFET and one side plate of input capacitance (2nd poly) as shown in Fig. 10. Furthermore, the parasitic capacitances were equalized using the parasitic extraction of the mask layout CAD tools. The results are listed in Table 3. The chip area shown in Fig. 9 is 131μm×101μm.

5. Conclusion

In this paper, a low-voltage and high-CMRR differential amplifier using FG-MOSFET's has been proposed. The proposed circuit has very high CMRR compared with the conventional one. Compared Monsurrò's differential amplifier, low-boost circuit, clock generator for low-boost circuit and twin-well process are not necessary. The proposed differential amplifier can be utilized in various analog signal process-

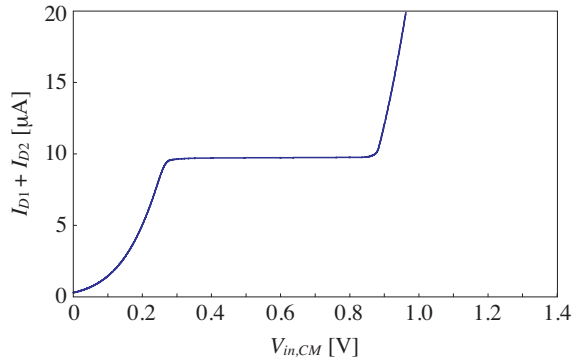

Figure 4. The relation between $I_{d1} + I_{d2}$ and $V_{in,CM}$.

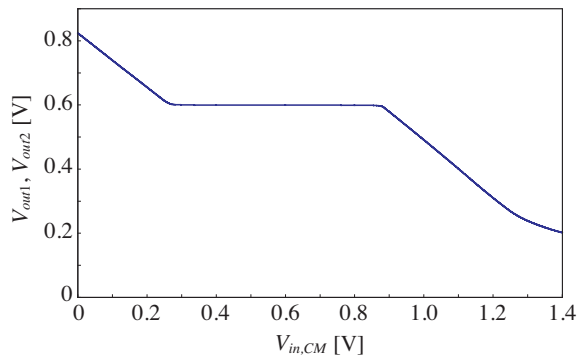

Figure 5. The relation between V_{out1}, V_{out2} and $V_{in,CM}$.

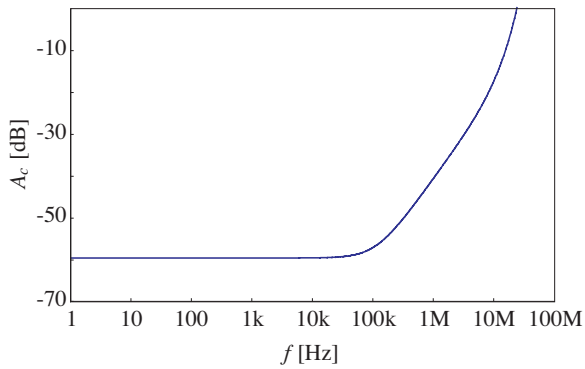

Figure 6. The relation between A_c and frequency (f).

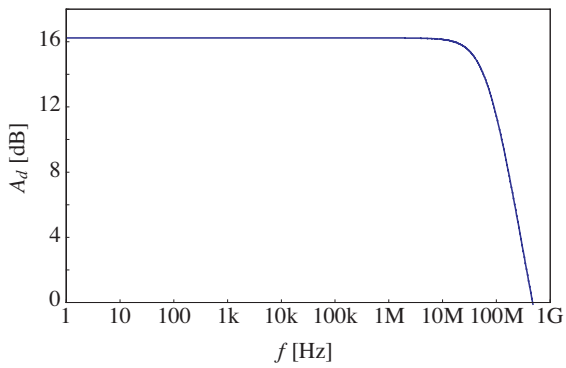

Figure 7. The relation between A_d and frequency (f).

Table 2. Simulation results

	Conventional		Proposed
	with I_{tail}	without I_{tail}	
V_{DD} [V]	2.0	1.4	1.4
A_d [dB]	20.2	21.1	16.2
A_c [dB]	−43.9	2.3	−59.5
CMRR [dB]	64.1	18.9	75.7
bandwidth [MHz]	70.9	71.6	71.5
current consumption [μA]	9.88	11.32	29.1
amplitude of V_{out} [V]	1.12	0.49	1.07

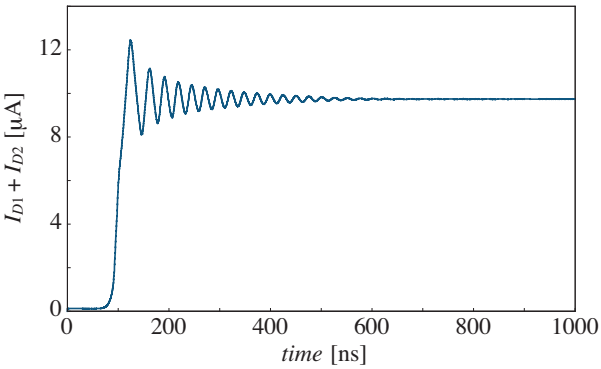

Figure 8. The simulation results of the start-up time.

Table 3. The parasitic capacitances of FG-MOSFET's.

FG-MOSFET	Parasitic capacitance	Value [fF]
M_1, M_{1r}	gate – substrate	0.20
	metal-wires – substrate	15.28
M_2, M_{2r}	gate – substrate	0.20
	metal-wires – substrate	15.27

ing LSI's operated at low power supply voltage.

Acknowledgment

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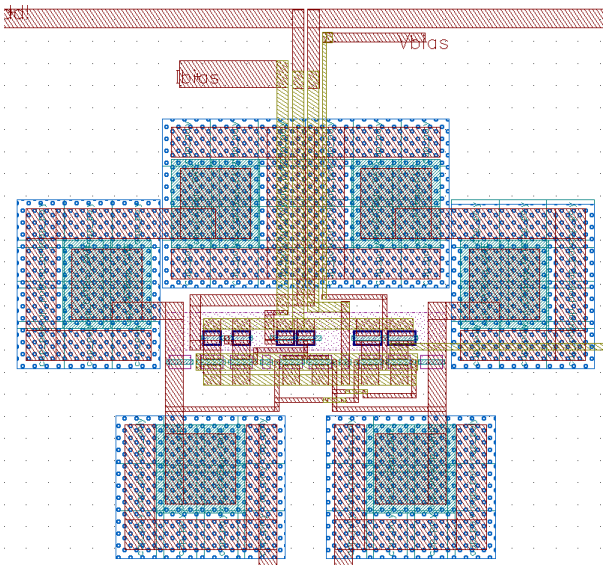

Figure 9. The layout of the proposed differential amplifier.

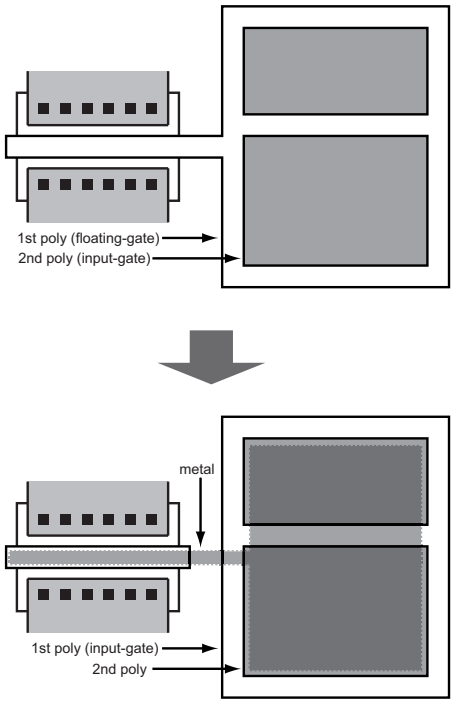

Figure 10. The layout of FG-MOSFET considering the parasitic capacitance between floating-gate and substrate.