The Implementation of Multiprocessor SoC for Industrial Wireless LAN Systems

Yushi Matsunaga, Mitsuru Hamada, Nico Surantha, Yuhei Nagao, Masayuki Kurosaki and Hiroshi Ochi
Department of Computer Engineering, Kyushu Institute of Technology
680-4 Iizuka Fukuoka 820-8502, Japan
E-mail : { matsunaga, hamada, nico, nagao, kurosaki, ochi } @dsp.cse.kyutech.ac.jp

Abstract: In this paper, an industrial Wireless Local Area Network (iWLAN) system to control industrial robots (iRBs) in factory automation (FA) environments is addressed. To improve the real-time property, we propose a multiprocessor architecture for iWLAN. Verification results on FPGA platform shows that our proposed schemes can improve real-time property of conventional iWLAN systems.

1. Introduction

In recent years, wireless technology has emerged as a promising alternative for industrial communication because it can provide the exibility needed for mobile robot settings. The wireless technology also is an advantage for the FA systems by reducing the cable connectivity and maintenance costs[1]. There are several solutions for FA wireless communication[2][3][4]. The disadvantage of these wireless communication systems is the poor throughput and real-time property. In particular, when the number of iRBs in FA system is large, the duration for one round of all iRBs communications can increase significantly. Therefore, it causes real-time control failure[5]. In order to mitigate these problems of the current FA systems, we have proposed a novel iWLAN system[5].

In industrial communication system, real-time property is important to achieve the safety system. For example, there is a strict requirement for interrupt response (in order of microseconds)[6]. In some cases, failure to do so could result in serious production failure. In real-time system, The real-time tasks handle external interrupts, either via register polling or interrupt servicing, that occur on the order of microseconds, i.e., to respond to the interrupt, to move the necessary data associated with each interrupt, to do computation and return the results before the next interrupt occurs[6].

In this paper, we propose a multiprocessor SoC architecture with asymmetric multiprocessor (AMP) to improve real-time property of iWLAN system. AMP architecture separate real-time and non real-time task on different processors

We perform verification on FPGA platform that contains dual processor. As a result, it shows that multiprocessor with AMP architecture produces better performance than single processor architecture for real-time property.

2. Industrial Wireless LAN Systems

2.1 iWLAN system

In this section, we explain about iWLAN for FA system. In Figure 1, we show that the system model of our proposed iWLAN system. Access Point (AP) is installed to MS and Station (STA) is installed to iRB. AP communicates to STA in wireless and transmit the orders of MS to IRB by a transmission protocol at the media access control (MAC) layer and a transmission technique at the physical (PHY) layer. In FA communication systems, the control data, which are transmitted between MS and iRBs. The transmission bandwidth is 80 MHz. In FA communication systems, the control data, which are transmitted between MS and iRBs, are short in length. Therefore, in this paper the control data of 32 octets in length are considered. The FA wireless communication system supports the deterministic transmission feature, in which the communications from MS to each iRB are in equal portions and in circular order without priority.

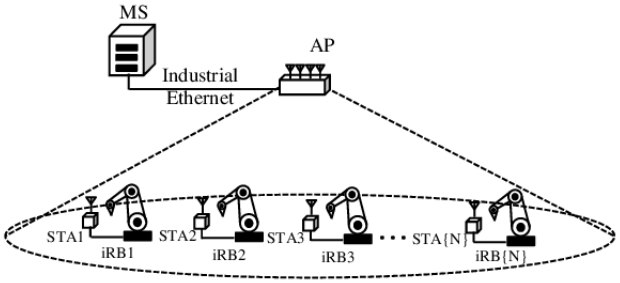

Figure 1. Proposed iWLAN System Model

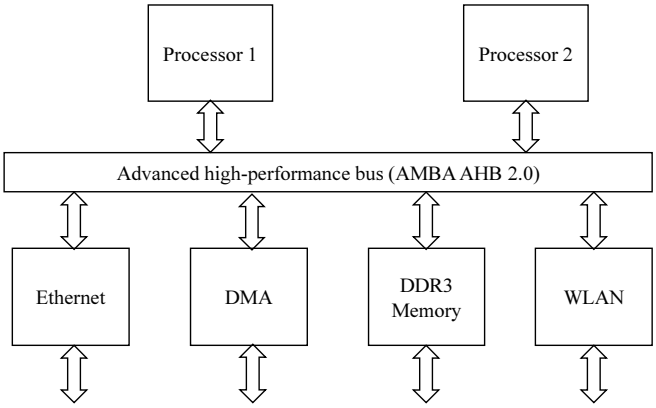

Figure 2. SoC architecture

2.2 iWLAN SoC architecture

The system design of the SoC of iWLAN is illustrated by Figure 2. It contains dual processors, an advanced high-performance bus (AHB) of advanced microcontroller bus architecture (AMBA), an Ethernet, a SDIO, a DMA and WLAN modules etc. Dual processors and DMA are aimed to speed up the performance of the system by distributing the tasks in the system e.g., a processor for peripheral transfers data and another one for WLAN operation.

The AHB acts as a high-performance system backbone bus. The high performance is achieved by pipelined opera-

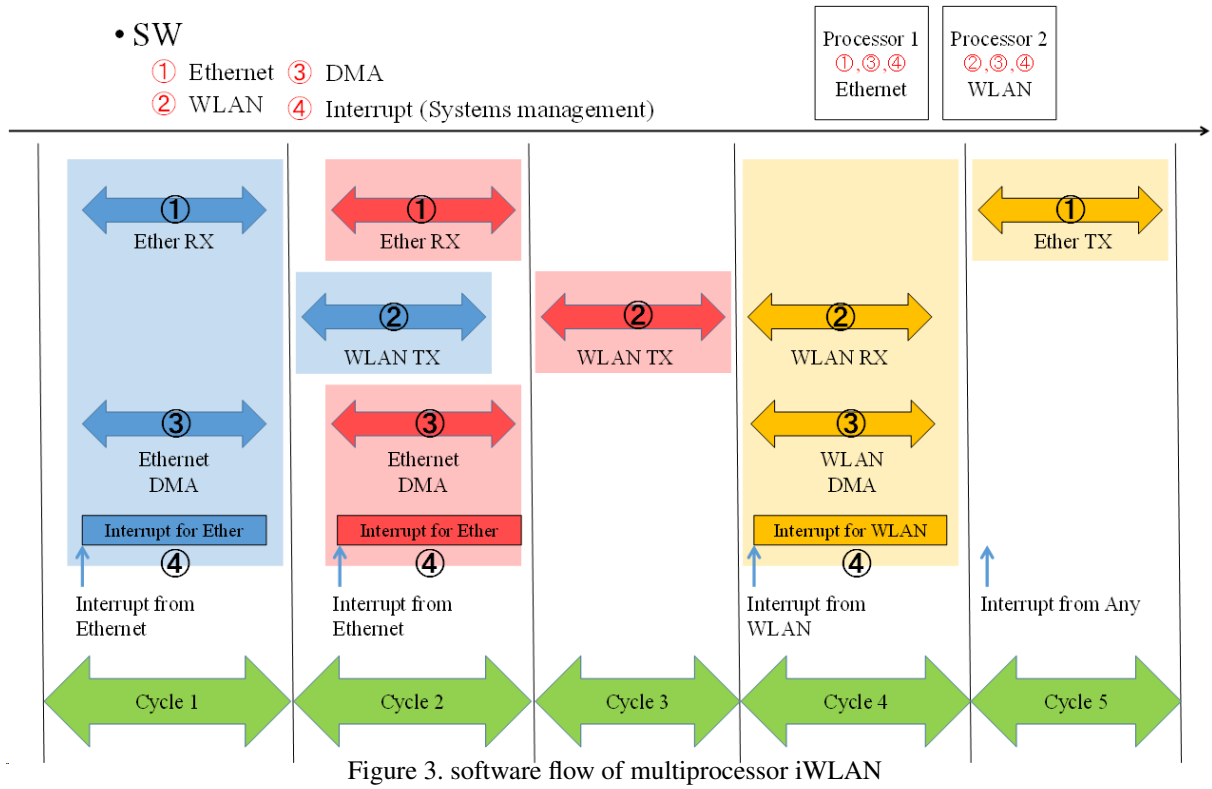

Figure 3. software flow of multiprocessor iWLAN

tion that overlaps arbitration, address and data phases. AHB is a multi- master bus that operates on single clock edge. As a consequence of this it can support the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripheral macrocell functions.

3. Multiprocessor of iWLAN System

There are two kinds of multiprocessor architecture, i.e. symmetric multiprocessor (SMP) and AMP systems[6]. In AMP architecture, individual processors can be dedicated to specific tasks and not all processors are treated equally. In SMP architecture, all processor execute a single operating system and are treated equally.

In iWLAN system, we have few bare metal applications, e.g. Ethernet, WLAN, DMA, interrupt and etc. In order to achieve real-time property, we want to create simple, light and fast system. Without utilizing operating system, we implement every bare metal application directly into two processors. Since Ethernet and iWLAN contain interrupt function that requires real-time response, we implement them into different processor.

In Figure 3, we show that iWLAN processing on dual processor. In cycle 1, processor 1 gets interrupt from Ethernet hardware, then it runs Ethernet and DMA software to transfer data from Ethernet to WLAN memory. In cycle 2, processor 2 runs WLAN data transmission and processor 1 gets another interrupt from Ethernet hardware and run the same process as cycle 1. In cycle 3, processor 1 runs WLAN data transmission. In cycle 4, it is another case when processor 2 gets interrupt from WLAN hardware, then it will transfer data from WLAN memory to Ethernet and perform data transmission. In cycle 5, processor 2 runs Ethernet data transmission. In case of single processor, the interrupt of iWLAN and Ethernet can not be process in parallel. Therefore, single processor has lower real-time property than dual processor.

4. FPGA Implementation

In Figure 4, we introduce our advanced FPGA verification platform. The motherboard contains Stratix IV 820 FPGA that can support up to 8.2 million gates of ASIC prototype. This is shown Table 1. In Table 2, the daughter board (Zynq-7030) has dual processor of ARM Cortex-A9 MPCore[7]. The FPGA in mother board can support full network layer design of iWLAN. The MAC layer software will be mainly implemented on daughter board. The baseband portion of PHY layer and part of MAC layer hardware will be implementation on main FPGA chip of motherboard. Furthermore, the motherboard can support many SoC peripheral configuration through the built-in peripheral or extension Zynq board, e.g. UART, Ethernet, USB, DDR3 memory, flash memory, etc.

5. Verification

In this section, we show the performance of single processor and AMP based multiprocessor. We compared the transmission time and the count value between both implementation to evaluate the performance and real-time property.

5.1 Verification Procedure

In Figure 5, we show the procedure of multiprocessor performance evaluation. In multiprocessor architecture, processor 1 runs the Ethernet application. In processor 2, we replace iWLAN software with count software to measure per-

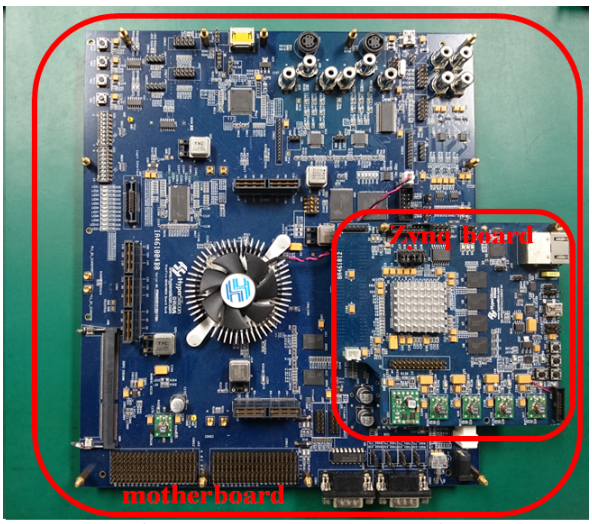

Figure 4. FPGA Implementation

Table 1. mother board configuration

Name	Specification
Device	StarFire-M820
FPGA	Stratix IV
number of LEs	813.05K

formance of every architecture. In single processor, Ethernet application and count application are alternately repeated. The processing time of single processor and dual processor are made equal. In Table 3, frequency of single processor is 400 MHz and it of dual processor is 200 MHz

5.2 Response Time Simulation

The real-time tasks handle external interrupts, either via register polling or interrupt servicing, that occur on the order of microseconds, i.e., to respond to the interrupt, to move the necessary data associated with each interrupt, to do computation and return the results before the next interrupt occurs. Real-time response time is typically expressed in terms of a real-time loop during which the system has to handle an polling and perform all the requisite computing before the next polling arrives. In Figure 6, we show that Ethernet application flow timing chart. A processor send Polling data to DDR3 memory. To respond to the polling, to transmit the Ethernet data associated with each polling, to do calculation transmission time and return the results before the next polling occurs. Ethernet application follows the following procedure. First, a processor create Ethernet packets to DDR3 memory. Second, a DMA transmits Ethernet packets to Ethernet and loop back to DDR3 memory. Last, a processor calculate transmission time. In this paper, we definition response time that from starting Margin for jitter to finishing Data Transmission. In Figure 7, it shows that dual processor architecture is more fast transmission time than single processor architecture. Therefore, dual processor architecture produces better real-taime property than single processor architecture.

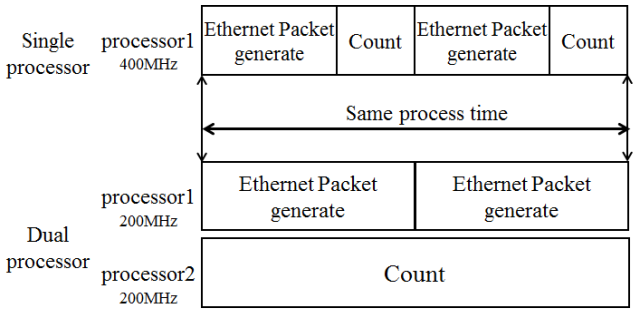

Figure 5. verification procedure

Table 2. daughter board configuration

Name	Specification
Device	Zynq-7030
FPGA	Kintex-7
Logic Cell	125 [KCells]
Block RAM	1060 [KB]
CPU	ARM Cortex-A9 MPCore
Number of Processor	2
on chip memory	256 [KB]
Ethernet	100 [MHz]
DDR	533.3 [MHz]

Table 3. processor frequency

processor	frequency
single processor	400[MHz]
dual processor	200[MHz]

5.3 Processing Speed Simulation

In Figure 5, we replace iWLAN software with count software to measure performance of every architecture. Larger count identicates smaller processing times, which is one of the criteria of processing speed. In Figure 8, it shows that single processor architecture and dual processor architecture compare count value. Therefore, dual processor architecture produces better real-time property than single processor architecture.

6. Conclusion

In industrial communication system, the real-time property is important to achieve safety system. In some cases, failure to do so could result in serious product failure.

An AMP multiprocessor architecture for iWLAN system has been presented in this paper. The simulation results shows that AMP multiprocessor architecture can improve real-time property of conventional iWLAN system that is proposed in [5]. In Figure 7, dual processor is higher real-time property than single processor. Furthermore, dual processor is higher performance than single processor by Figure 8. Therefore, our architecture can achieve real-time property for iWLAN systems.

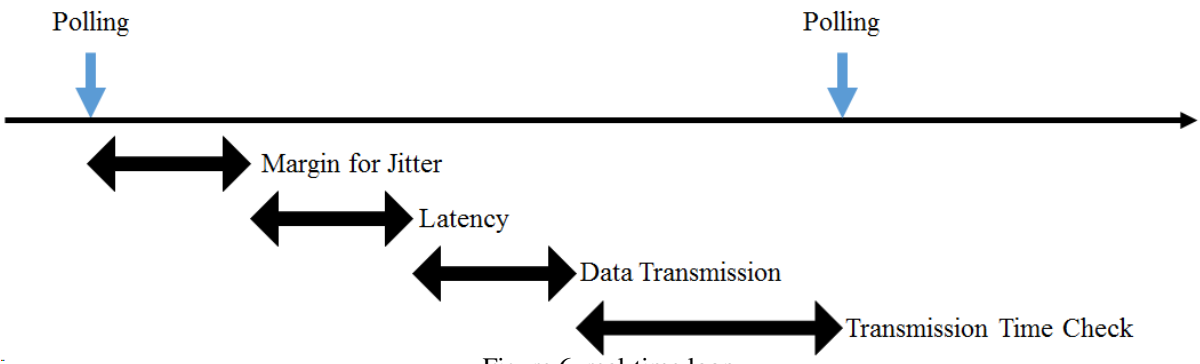

Figure 6. real-time loop

References

[1] A. Willig: Recent and Emerging Topics in Wireless Industrial Communications: A Selection;*IEEE Transactions on Industrial Informatics*, pp. 102–124 (2008)

[2] L. Lo Bello, O. Mirabella: Communication techniques and architectures for Bluetooth networks in industrial scenarios;*IEEE Conference on Emerging Technologies & Factory Automation (ETFA)*, pp. 52–61 (2005)

[3] D. Egan: The emergence of ZigBee in building automation and industrial control;*Computing and Control Engineering Journal*, Vol. 16, No. 2, pp. 14–19 (2005)

[4] N. Baker: ZigBee and Bluetooth strengths and weaknesses for industrial applications;*Computing and Control Engineering Journal*, Vol. 16, No. 2, pp. 20–25 (2005)

[5] Duc Khai Lam, et.al, "A Fast and Safe Industrial WLAN Communication Protocol for Factory Automation Control Systems," *ISCIE Transaction of the Institute of Systems, Control and Information Engineers*, Vol.29, No.1, Jan. 2016.

[6] Chee Nouk Phoon, et al, : Bare-Metal, RTOS, or Linux? Optimize Real-Time Performance with Altera SoCs, ALTERA White paper, WP-01245-1.0, December 2014

[7] Tatsumi Uwai, et al., "Live demonstration: IEEE802.11 wireless LAN system verification platform," Proc. 2014 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2014), pp.175-176, Ishigaki Island, Okinawa, Japan, November 17-20(18) 2014

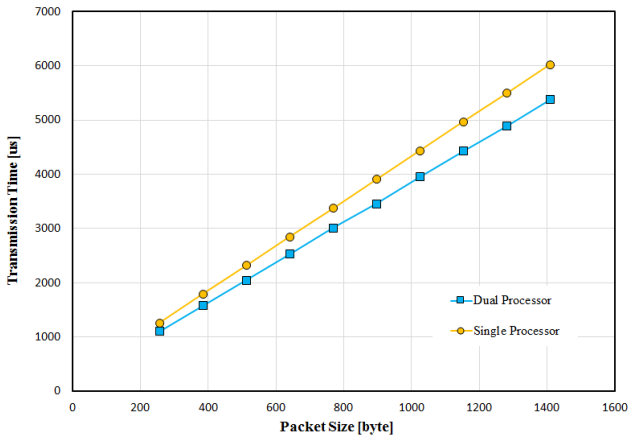

Figure 7. real-time result

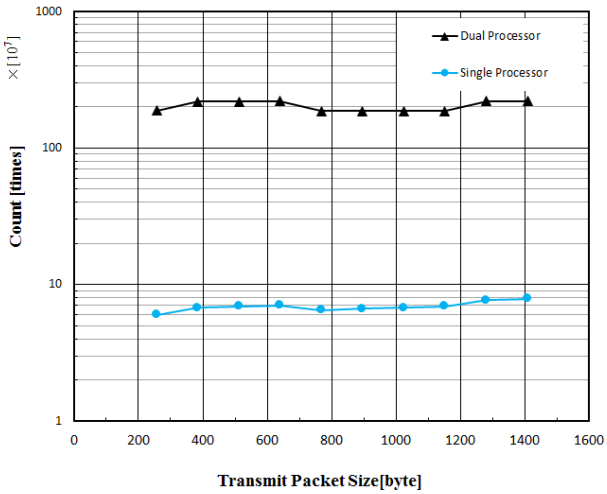

Figure 8. verification result