Low-Power 12-bit 160-MS/s Pipeline A/D Converters

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Abstract: Low-power 12-bit 160-MS/s pipeline A/D converters are designed for wireless receivers. Instead of using ultra-deep submicron devices of low supply voltage, we employ analog-option devices that operate at supply voltage of 2.5V in a 90-nm CMOS process. To achieve lower power dissipation, an I/Q amplifier sharing technique is employed. Furthermore, charge transfer level shifters are proposed in S/H circuits and MDACs for realizing class-AB operation.

The area is 1.1mm^2, the simulated power dissipation is 75mW/channel and the simulated ENOB is 11.15bit.

1. Introduction

In next-generation mobile communication terminals, high-resolution and high-speed Analog-to-Digital (A/D) converters are required for the higher data transfer rate. In addition, low power consumption is urgently required for battery-powered operation.

In a high-accuracy A/D converter, deep submicron technology does not necessarily correspond to low power. As the supply voltage becomes lower, the allowable signal swing becomes narrower. This results in the degradation of Signal-to-Noise Ratio (SNR). To satisfy the required SNR under the limited signal swing, the sampling capacitors must be increased to reduce the kT/C noise. This results in larger current consumption of the opamps. Since we can use a multi-supply process, one of the key points of low-power design is the selection of the optimum supply voltage.

Power for the amplifiers used in Sample-and-Hold (S/H) circuits and Multiplying Digital-to-Analog Converters (MDACs) dominates the A/D converter power dissipation. Therefore, we reduce the number of amplifiers by using an I/Q amplifier sharing technique. Although switched-capacitor level shifter for a class-AB opamp is effective to accomplish lower power, it is not preferable for the architecture of I/Q amplifier sharing. Hence, we propose a level shifter applicable to I/Q amplifier sharing to reduce the power consumption of opamps in 12-bit pipeline A/D converters.

2. Supply Voltage and Structure of Opamps for Low Power

It is important to select the optimum supply voltage and structure of opamps for low-power design. High supply voltage allows the large signal swing. Also, opamps have various structures. For example, a folded cascode opamp can achieve large signal swing but has high power consumption, and a telescopic opamp has low power

consumption but has narrow signal swing. In a pipeline A/D converter, large signal swing permits small sampling capacitance while keeping desired SNR. Small capacitances make the area small and the power consumption low. However, since we cannot use capacitances that are too small in view of the mismatch, supply voltage that is too high increases the power dissipation. In [1], a methodology to select the optimum supply voltage and structure of opamps used in S/H circuits and MDACs are introduced. In our specification, 2.5V and telescopic structure are derived for the lowest power. We achieve progress in terms of lower power consumption.

3. I/Q Amplifier Sharing

Fig 1 shows the block diagram of a direct-conversion receiver that has a quadrature demodulator (QDEM). Most of the recent receivers employ a QDEM that outputs an in-phase channel (I-channel) signal and a quadrature-phase channel (Q-channel) signal. In such a receiver, two A/D converters are used between the analog block and the digital block. For the power reduction, an I/Q amplifier sharing technique is employed [2]. Fig 2 shows the architecture of 12-bit I/Q amplifier sharing pipeline A/D converters with 2.5-bit/stage. The technique reduces the number of amplifiers to half that of the A/D converters. The opamps in a one-channel pipeline A/D converter normally have sampling phase and amplifying phase, and are idle in sampling phase. However, in I/Q amplifier sharing pipeline A/D converters, the opamps always operate for amplifying phases of I and Q channels.
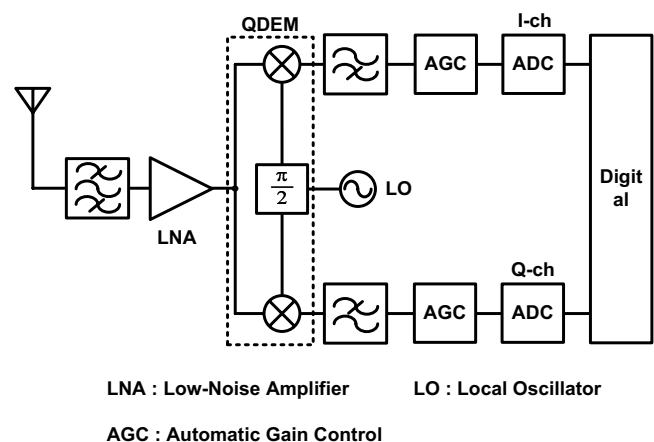

LNA : Low-Noise Amplifier   LO : Local Oscillator

AGC : Automatic Gain Control

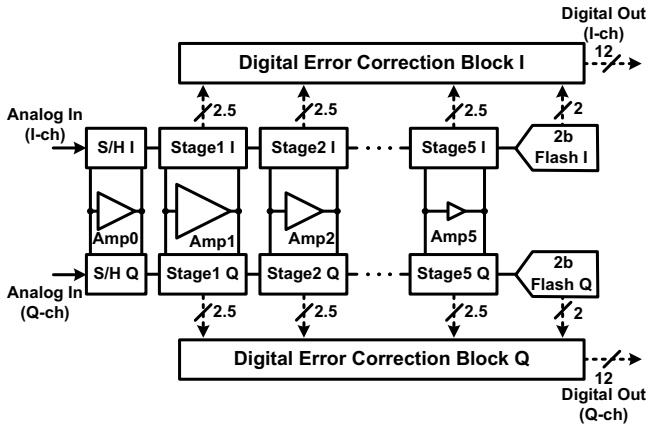Fig 1. Block Diagram of a Direct-Conversion Receiver

Fig 2. Architecture of pipeline A/D converters
with I/Q amplifier sharing

4. Class-AB Opamp with Charge Transfer Level Shifter

As mentioned in section 2, the structure of opamps in S/H circuits and MDACs is telescopic opamp using 2.5V transistors. Here we propose techniques for low-power opamp design.

4. 1 Charge Transfer Level Shifter

To accomplish the high slew rate and the large transconductance with low power dissipation, a class-AB telescopic opamp with switched-capacitor level shifter is conventionally proposed, as shown in Fig 3 [3]. The opamps in one-channel pipeline A/D converter normally have sampling phase and amplifying phase, and are idle in sampling phase. This conventional class-AB opamp utilizes the idling time. Capacitors C_{LS} are connected between the gate of NMOS input transistors (Mn1, Mn2) and the gate of PMOS current source (Mp1, Mp2). The terminals of C_{LS} are biased to the corresponding appropriate voltage, V_{com} and V_{bias}, while the opamp is idle in sampling phase. In amplifying phase, the switches are disconnected, and the differential input signal is applied to the input transistors. Then the gate voltages of Mp1 and Mp2 track the input. The timing chart is shown in Fig 5(a).

Fig 4 shows the transfer curve of one side of the fully differential amplifier [4]. When a large signal is applied to the inputs, one of the input transistors (for example, Mn1) becomes ON and the other (Mn2) becomes OFF. In the case of class-A telescopic opamp, the maximum output driving current is limited by Io/2, where Io is the tail current. On the other hand, in class-AB telescopic opamp, one of the PMOS current sources (Mp1) becomes OFF and the other (Mp2) remains ON since C_{LS} acts as a level shifter. Then the maximum output driving current is limited by Io instead of Io/2. Therefore, the slew rate and the transconductance of the class-AB telescopic opamp are doubled without increasing power dissipation, assuming the transconductance of NMOS and PMOS are the same. However, this configuration is not preferable for the architecture of I/Q amplifier
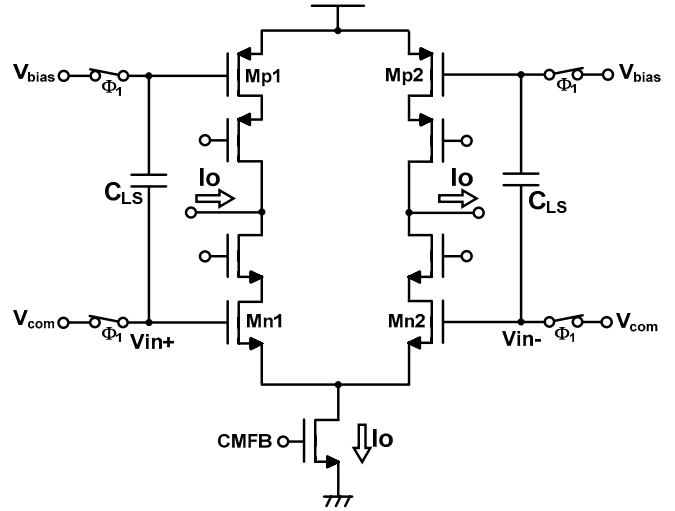

Fig 3. Conventional class-AB telescopic opamp
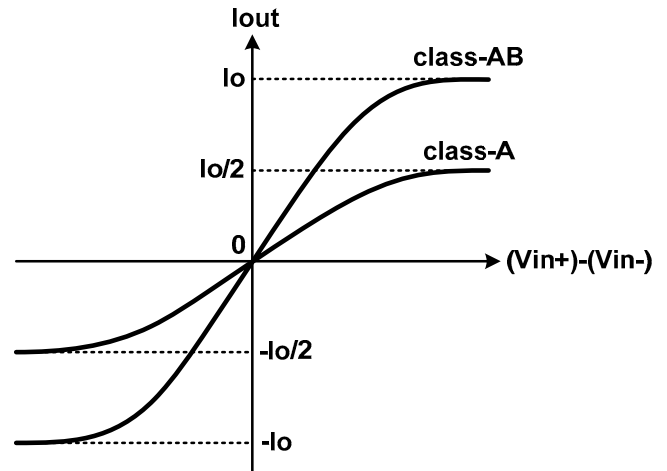with capacitor level shifter

Fig 4. Transfer curve of one side of amplifier

sharing because of the necessity of additional clock phase for charge C_{LS} before using opamps as shown in Fig 5(b). Since additional phase reduces amplifying time, higher speed is required for opamps.

To overcome this problem, we propose the class-AB telescopic opamp with charge transfer level shifter shown in Fig 6. Level shift capacitor C_{LS} is charged by charge transfer from precharge capacitors C_1 and C_2 connected between V_{bias} and V_{com} by switches. Fig 5(c) shows the timing chart of Φ_1 and Φ_2. C_1 and C_2 are precharged alternately. While C_1 is precharged, C_{LS} is charged by charge transfer from C_2, and *vice versa*. Finally, V_{bias}-V_{com} is copied across C_{LS} and C_{LS} acts as level shifter, resulting in class-AB operation of the telescopic opamp. Hence additional clock phases and higher-speed opamp are unnecessary. Of course, the power consumption of level shifter is very low because it is constructed of capacitors.
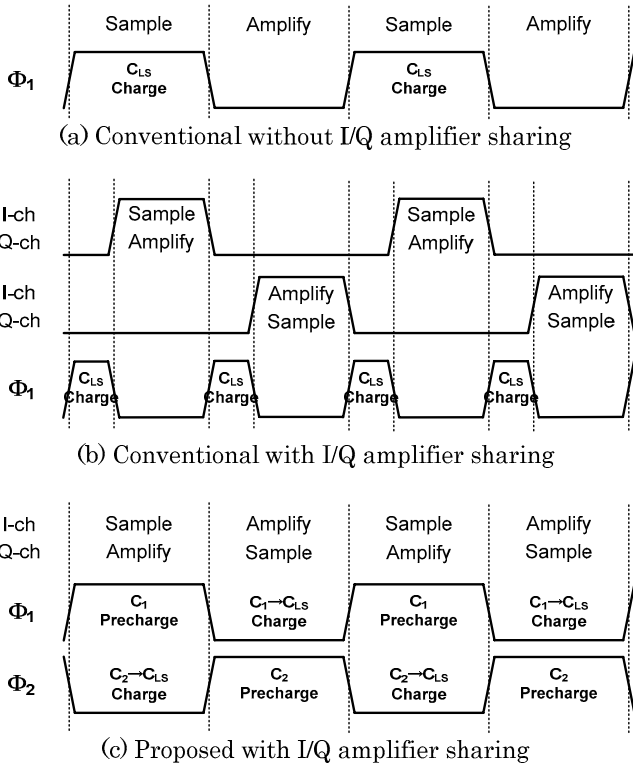
(a) Conventional without I/Q amplifier sharing

(b) Conventional with I/Q amplifier sharing

(c) Proposed with I/Q amplifier sharing

Fig 5. Timing Chart

4. 2 Gain-Boosting Amplifier with Charge Transfer Level Shifter

The opamp has gain-boosting amplifiers, Ap and An, for high gain. Conventionally, transimpedance amplifiers are used as gain-boosting amplifiers to achieve the large output signal swing [2]. However, their power consumption is high because of the configuration with current mirror.

Applying the above charge transfer level shifter to input of N-ch cascode amplifier, a simple common-source cascode amplifier can be used without reducing the output signal swing of the opamp, as shown in Fig 6. This reduces the power consumption to half that of a transimpedance amplifier because of the simple configuration. Furthermore, the N-ch common-source cascode amplifier with the input voltage level adjusted by level shifter can also be used for P-ch gain-boosting amplifier Ap. The N-ch common-source cascode amplifier has an advantage of speed over P-ch because of larger transconductance. This further reduces power dissipation compared with P-ch common-source cascode amplifier.

4. 3 Low-Voltage Input Transistors

To achieve lower power consumption, 1.2V transistors are used only for the input transistors of the opamp. That leads to large transconductance without increase of current.

5. Layout and Simulation Results

The layout of the 12-bit pipeline A/D converters designed in 2.5-V transistors as an analog option of 90-nm CMOS process is shown in Fig 7. The sampling frequency is 160MS/s. The area is $1.1mm^2$. In simulation, the total power consumption is 150mW, which corresponds to 75mW/channel. The simulated Effective Number Of Bits (ENOB) is 11.15bit.
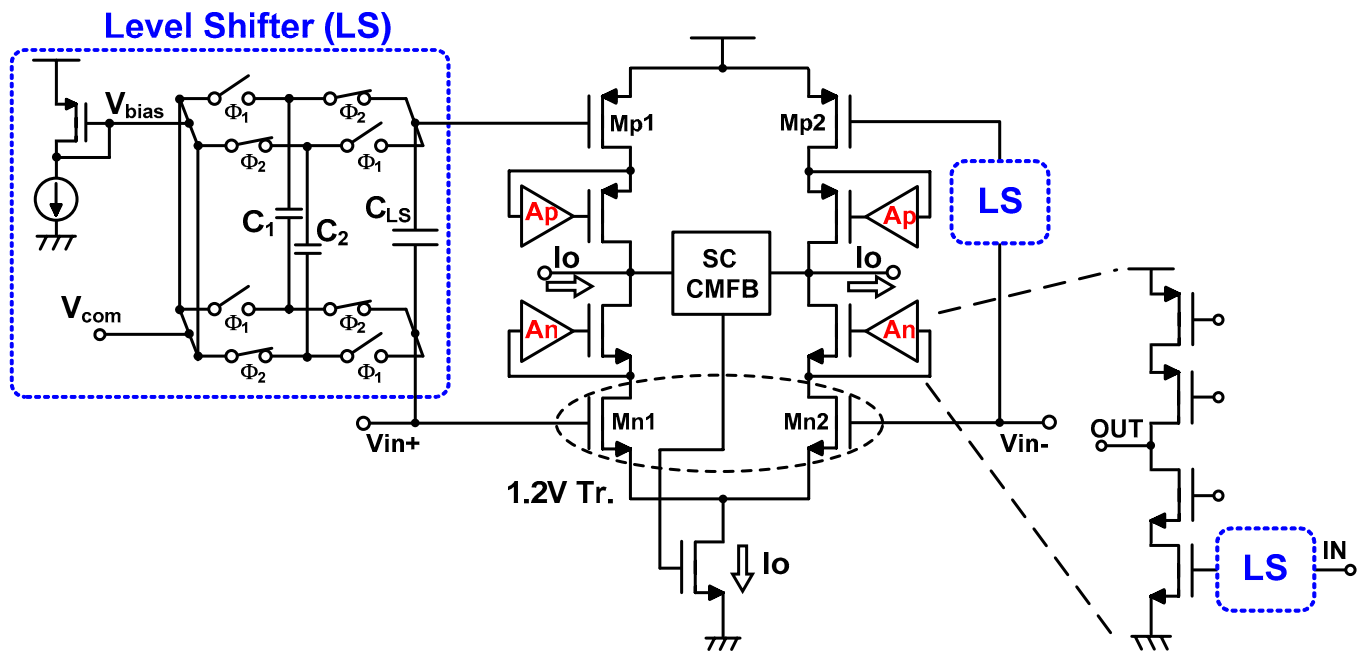

Fig 6. Proposed class-AB telescopic opamp with charge transfer level shifter

Table 1. Performance Comparison

|	This Work	Andersen [5]	Ito [6]	Iroaga [7]	Grace [8]
Sampling Rate	160 MS/s	110 MS/s	100 MS/s	75 MS/s	80 MS/s
Process	90-nm CMOS (Analog 2.5-V transistor)	0.18-μmCMOS	90-nmCMOS	0.35-μmCMOS	0.25-μmCMOS
Supply Voltage	Analog 2.5 V / Digital 1.2 V	1.8 V	1.2 V	3 V	2.5 V
ENOB	11.2 bit	10.4 bit	9.63 bit	10.6 bit	11.8 bit
Power	75 mW/ch	97 mW	55 mW/ch	273 mW	755 mW
FoM	0.2 pJ/conv.	0.65 pJ/conv.	0.69 pJ/conv.	2.35 pJ/conv.	2.65 pJ/conv.
Area	1.1 mm^2 (2ch)	0.86 mm^2	5.78 mm^2 (2ch)	7.9 mm^2	22.6 mm^2
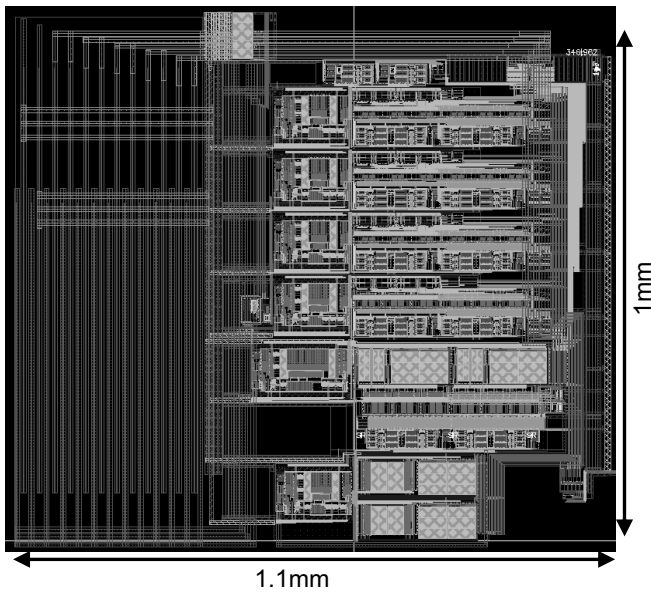
Fig 7. Layout

Table 1 compares the performance with that of the previously reported 12-bit pipeline A/D converters with a conversion speed of around 100MS/s. Figure of Merit (FoM) is defined by

$$FoM = \frac{P}{f_{samp} 2^{ENOB}} \quad [\text{J/conv.}]$$

where f_{samp} is sampling frequency and P is power dissipation.

From Table 1, this work shows the best FoM with the smallest area of all A/D converters.

6. Conclusions

For next-generation wireless receivers, a 12-bit 160-MS/s pipeline A/D converter with 2.5-bit/stage was designed in 2.5V transistors as an analog option of 90-nm CMOS process. For low power dissipation, an I/Q amplifier sharing technique is employed. In addition, charge transfer level shifters are proposed in S/H circuits and MDACs for class-AB operation. It is applicable to I/Q amplifier sharing. Furthermore, large transconductance is achieved with 1.2-V input transistors of the opamp.

The area is 1.1mm^2, the simulated power dissipation is 150mW, which corresponds to 75mW/channel, and the simulated ENOB is 11.15bit. The best FoM A/D converter has been achieved with the smallest area.

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