Proposal of a Hardware Task Engine To Improve Realtime of an Interrupt Handling

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Absract: In this paper, hardware called a hardware task engine is proposed to achieve embedded controller architecture for signal processing. An interrupt task that is highest priority and executes a signal processing is executed a hardware task engine. A hardware task engine works highly realtime, because of it has high-speed and flexible processing ability, and it reduces start up delay from interrupt signal. A prototype of a hardware task engine is made FPGA, and is evaluated on actual magnetic encoder. Start up delay from interrupt signal of a hardware task is 41.60 nanoseconds, and it is faster than software by 3.0 times at a half clock frequency, and temperature rise is reduced to 13.4%. As a result, we can corroborate availability of a hardware task engine.

1. Introduction

An embedded controller to control a servo motor is required high speed performance, because motion of controlled objects is increasingly speeding up. Concurrently, a signal processing of encoder to acquire feedback information is required highly realtime. In signal processing of an encoder, acquiring sensor data and signal processing, communication processing to servo drive is implemented by interrupt handling. Typically, a signal processing of encoder is corresponded into software using a high performance CPU or DSP. Start up delay from interrupt signal has a bad effect of hard realtime. But, using a high performance CPU and DSP can't solve problem of start up delay from interrupt signal. Further, speeding up of clock frequency has another problem that is temperature rise.

2. A magnetic encoder

2.1 A magnetic encoder processing

Fig1 is a block diagram of a magnetic encoder system. A magnetic encoder is a position sensor to calculate rotating angle to use information from a magnetic sensor. And it is mounted back end of a servo motor. Output signals from a magnetic encoder inputs to analog front end of a magnetic encoder interface board, thereafter it is converted to a digital signal. Subsequently, a digital processing unit in CPU executes signal processing of a magnetic encoder. At first, digital processing unit executes data reading processing to read a conversion data from analog front end. Next, getting data is executed data correction processing such as offset correction. A rotating angle is made angle calculation processing to use a corrected data. Finally, calculated a rotating angle is written communication data writing processing to communication LSI. Thereafter, it is sent to servo drive. In a digital processing unit, processing of a magnetic encoder called a normal processing is performed on interrupt handling.

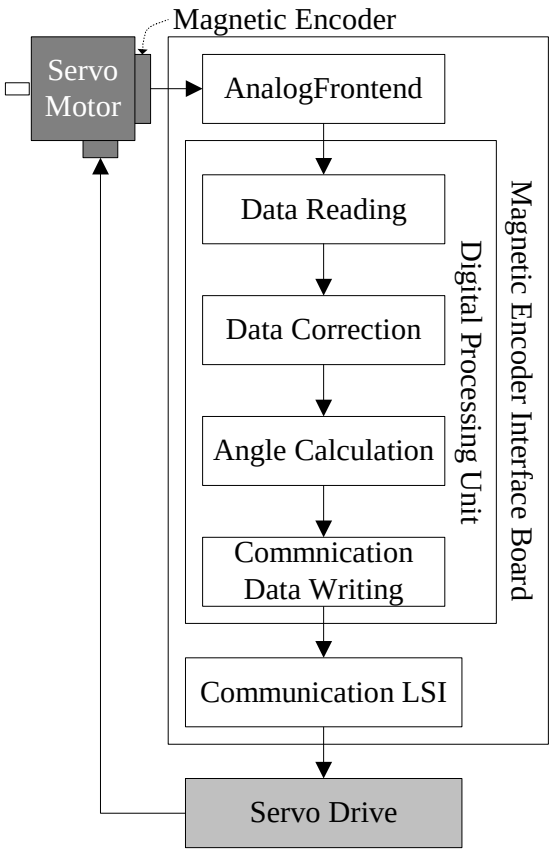

Fig1. A block diagram of a magnetic encoder system

2.2 evaluation of software

A normal processing is evaluated a magnetic encoder evaluation board that use a V850E/MA1 CPU. Operating frequency of a V850E/MA1 CPU is 48 MHz. A normal

processing time to execute by a V850E/MA1 CPU is 34.79 microseconds. Further, at room air temperature is 25 degrees centigrade, temperature rise to execute a V850E/MA1 CPU is 26.2 degrees centigrade.

3. A hardware task engine

3.1 A Hardware task

In this paper, hardware called a hardware task engine[1] is proposed to achive high perfomance and lower frequency for embedded controllers such as rotary encoder. A hardware task engine is hardware for embedded controllers with highly realtime. Because of having high speed and adaptable processing ability, and reducing start up delay from interrupt signal. A hardware task is defined hardware that can do cooperation action between an execution unit and peripheral units to relate with an execution unit.

3.2 A hardware task engine

A hardware task engine is shown in Fig.2.

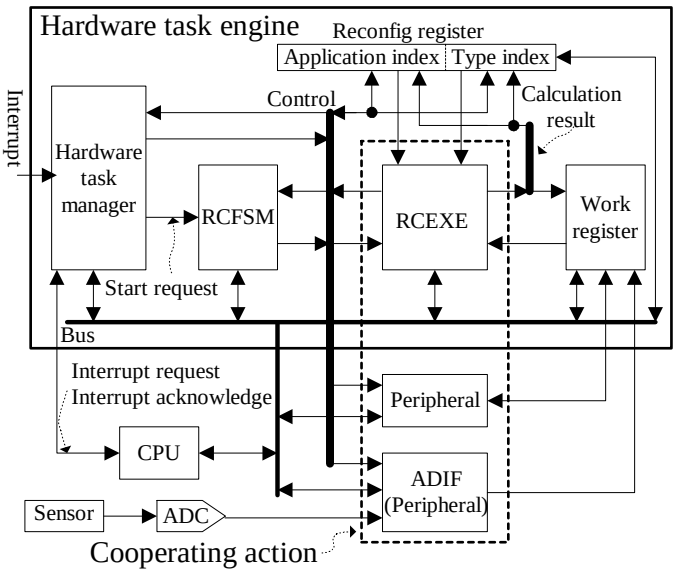

Fig2. A hardware task engine block diagram

A hardware task engine consist of a RCEXE (ReConfigurable EXEcution unit) that is dynamic reconfigurable data path and a RCFSM (ReConfigurable Finite State Machine unit) that is reconfigurable finite state machine, a reconfig register to indicate reconfiguration about a RCEXE, a hardware task manager, a work register. A hardware task is realized to cooperate both a RCEXE and peripheral units to relate with it. A cooperating action of a hardware task is controlled by a RCFSM to reconfigure a state transition. RCFSM is sequential circuit of moore type, can reconfigure both state transition and output signals. Therefore, RCFSM can control sequence of a hardware task. Further, RCEXE can reconfigure contents of signal processing. Because of above reasons, a hardware task engine can correspond to various signal processing. So, a hardware task has flexibility such as software. A hardware task reduces start up delay from interrupt signal, because a hardware task manager manages a starting up it. A hardware task manager is controller that is based priority encoder, it manages a interrupt signal and starts up hardware tasks. A work register is use processing of RCEXE. And is can access from CPU. Some registers of peripheral units are allocated into a work register to cooperate with a RCEXE. A reconfig register is consists of two index that is called application index and type index. Interacting an application index, RCEXE is reconfigured framework that adapts selected application. Interacting a type index, RCEXE is decided a function and network of framework.

4. Evaluation result

4.1 A hardware Task engine evaluation board

A hardware task engine is adapted to magnetic encoder processing. Data reading processing and calculating angle processing is implemented in hardware. A communication data writing processing is left software processing, because of being mainly composed of alarm processing. A hardware task is realized to cooperate with hardware task engine and their. Using FPGA (Field Programmable Gate Array), SoC is designed to use an adapted hardware task engine. FPGA is a Stratix(EP1S40) that is Altera Corporation product. FPGA block diagram is shown in Fig3.

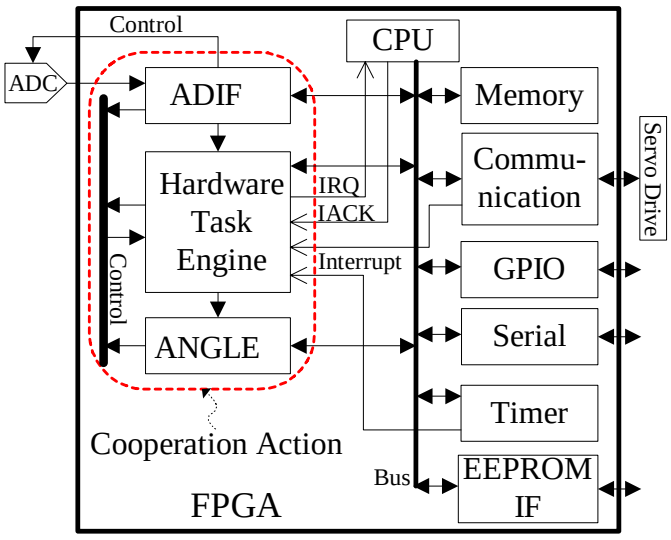

Fig3. FPGA block diagram

Into a FPGA, there is a hardware task engine and CPU, memory, several peripheral units. Peripheral units to relate with a RCEXE are an ADIF and an ANGLE. An ADIF is

data reading that implements in hardware. An ANGLE is angle calculation that implements in hardware. Because of using C compiler, CPU is made use of an Aquarius[2] CPU that is 32bit soft macro processor. Operating frequency of both a hardware task engine and an Aquarius CPU is 24 MHz. FPGA can control clock to supply, because of implementing a gated clock. To evaluate basic properties of a hardware task engine, a magnetic encoder evaluation board is made to use a FPGA. A magnetic encoder evaluation board is shown in Fig4. An application to evaluate a hardware task engine is made use of signal processing of a magnetic encoder.

Fig4. A magnetic encoder evaluation board

A hardware task is confirmed to reconfigure to signal processing of a magnetic encoder. Moreover, Executing signal processing of a magnetic encoder on a hardware task engine is confirmed to use an AC servo motor.

4.2 Start up delay

Start up delay from interrupt signal is made a compare between a hardware task engine and software processing. In a hardware task engine, start up delay from interrupt signal is 41.60 nanoseconds, as shown in a Fig.5. As a result, a hardware task engine can be reduced to 0.037 times at a half clock frequency.

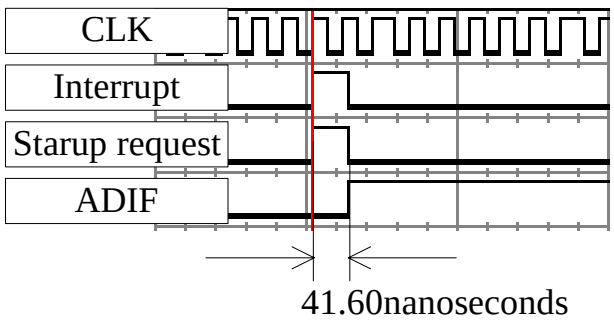

Fig5. Start up delay from interrupt signal

4.3 Processing time

Processing time of interrupt handling is made a compare between a hardware task engine and software processing. In a hardware task engine, a processing time of interrupt handling is 11.44 microseconds, as shown in a Fig.6. As a result, a hardware task engine can be speed up 3.0 times at a half clock frequency.

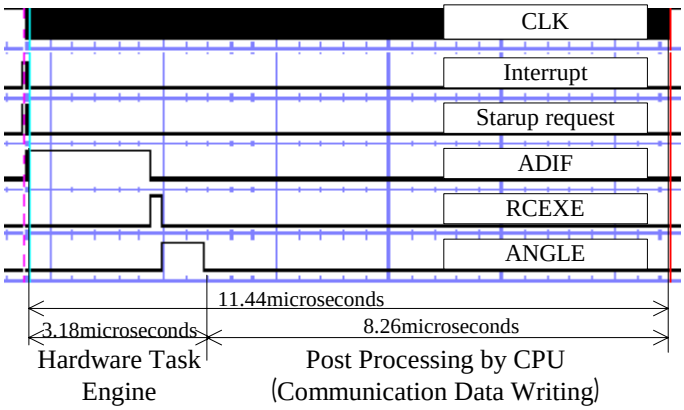

Fig6. Processing time of a hardware task engine

4.4 Temperature rise

Temperature rise is made a compare between a hardware task engine and software processing. At room air temperature is 25 degrees centigrade, temperature rise is 3.5 degrees centigrade with a clock gating. And, in the same condition, temperature rise is 4.7 degrees centigrade without a clock gating. It is shown in a Fig.7. As a result, a hardware task engine can be reduced to 13.4% at a half clock frequency.

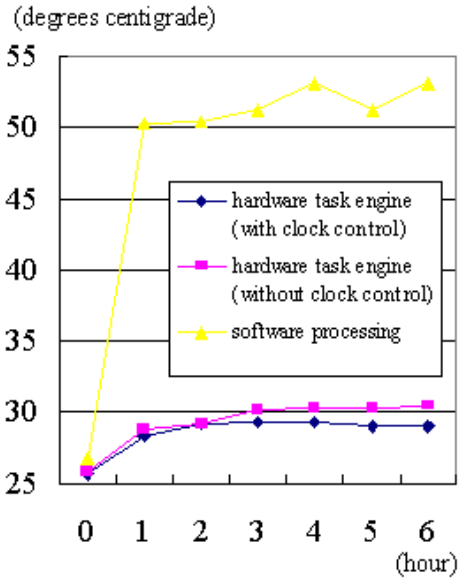

Fig7. Temperature rise

5. Conclusion

In this paper, hardware called a hardware task engine is proposed to achieve high speed and lower frequency for embedded controllers. An interrupt handling that is highest priority and executes a signal processing is executed a hardware task engine. A hardware task engine works highly realtime, because it has high speed and adaptable processing ability, and it reduces start up delay from interrupt signal. A prototype of a hardware task engine is made a FPGA, and is evaluated by actual magnetic encoder with magnetic sensors. Start up delay from interrupt of a hardware task is 41.60 nanoseconds, and it is faster than software by 3.0 times at a half clock frequency, and temperature rise is reduced to 13.4%. As a result, we can corroborate availability of a hardware task engine.

References

[1] Y.Kashiwagi, N.Yamauchi, and T.Sakata, "Proposal of a Hardware Task Engine and Design, Prototype Fabrication and Evaluation of a Sensor Signal Processing SoC Using it", SICE Journal of Control, Measurement, and System Integration, Vol.44, No2, pp.107-114, 2008

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