

An Interface based on Switched-Capacitor Sample/Hold circuit of Differential Capacitance Transducers

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Abstract: For high-accuracy and high-speed signal processing of differential capacitance transducers, an interface circuitry based on a switched-capacitor sample/hold circuit using unity-gain buffer (UGB) is developed. The interface produces the output voltage which is proportional to the ratio of difference-to-sum of two capacitors of a differential transducer using only single reference voltage, V_r . Hspice simulations are described to predict performances of the interface when implemented by 0.35 μm n-well CMOS process. Experimental results using discrete components are also given to confirm the principles of operation.

1. Introduction

A differential capacitance transducer consisting of two capacitors is widely used to detect such physical quantities as pressure difference, linear displacement, acceleration, and rotational angle [1]. It can be represented electrically by two capacitors, C_a and C_b , whose capacitances change complementarily with a measurand. Its electrical equivalent, which includes parasitic capacitances C_{pa} , C_{pb} , and C_{pc} , is shown in Fig. 1. In a rotational angle encoder, C_a and C_b , change linearly with the angle x .

$$C_{a,b} = \frac{C_o}{2} (1 \pm x), \quad (1)$$

where $C_o = C_a + C_b$ is the total capacitance. In pressure transducers, on the other hand, C_a and C_b change hyperbolically with applied pressure x [2]:

$$C_{a,b} = \frac{C_o}{2} \frac{1}{1 \pm x}. \quad (2)$$

In either case, the measurand x can be detected independently of the total capacitance by the following ratiometric operation, that divides the capacitance difference by its sum [3]

$$x = \frac{C_a - C_b}{C_a + C_b}. \quad (3)$$

Besides the linear extraction of a measurand x , the ratiometric operation is effective for canceling capacitance changes due to temperature.

Several methods have so far been proposed for the ratiometric operation, including the feedback control of the excitation [4], [5], relaxation oscillation using integration and differentiation [6], and switched-capacitor (SC) charge-

balancing analog-to-digital (A/D) conversion [7], and oversampling $\Delta\Sigma$ modulating [8], [9].

A CMOS interface for high-speed ratiometric operation is highly requested by differential capacitance transducers for acceleration and rotary angle measurements. To respond the request, an interface has been proposed based on a SC sample/hold (S/H) circuit [10]. The architecture is simple and also suited for micromachined differential capacitance transducers. Its accuracy is, however, limited by the charge injection due to clock feedthrough accompanying a CMOS analog switch.

A new interface is developed based on switched-capacitor (SC) sample/hold (S/H) circuit using unity-gain buffer (UGB) and that can compensate the effect of the charge injection. The circuit requires only single reference voltage, V_r , for the ratiometric operation. This paper describes its configuration, simulated performances by HSPICE using a 0.35 μm n-well CMOS process parameter, and experimental results using discrete components.

2. Interface

Fig. 2(a) shows a circuit diagram of the interface, where C_a and C_b represent two capacitors of a difference capacitance transducer. The switching sequence is shown in Fig. 2(b). In the $\phi_1 = \phi_2 = \phi_3 = "1"$ phase, C_a is charged to a reference dc voltage V_r and C_b discharged. In the next $\phi_1 = \phi_2 = \phi_3 = "0"$ phase, two capacitors are connected in parallel, to produce the output voltage V_{o1} :

$$V_{o1} = \frac{C_a}{C_a + C_b} V_r. \quad (4)$$

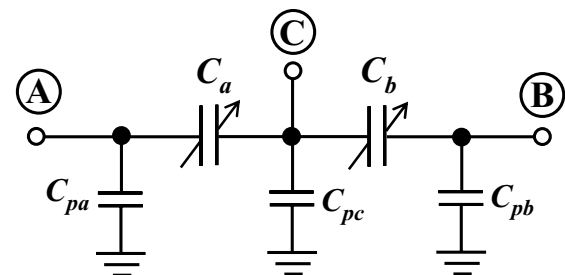


Fig. 1. An equivalent circuit of a differential capacitance transducer

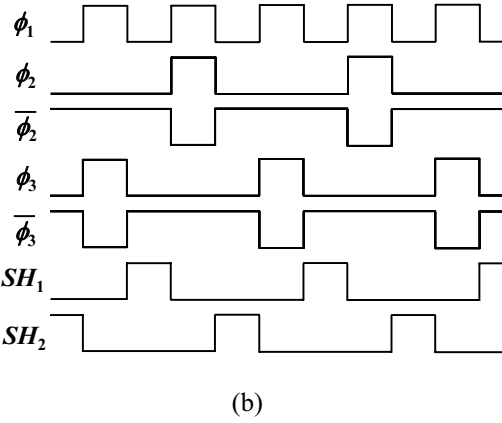
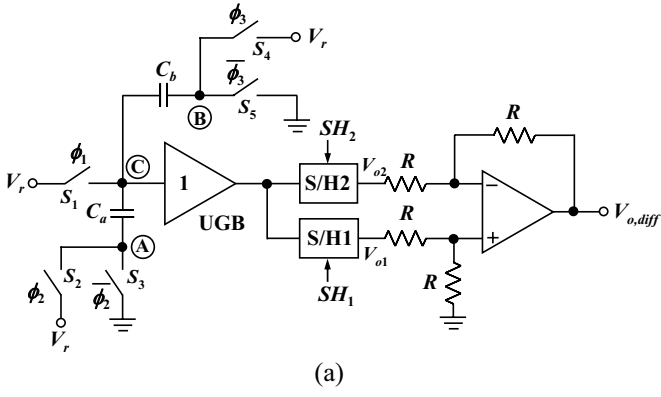


Fig. 2. (a) Circuit diagram of the interface.
(b) Switching sequence.

In this $SH_1=1$ phase, Sample/Hold (S/H) 1 circuit samples V_{o1} . In the $\phi_1 = \phi_2 = \phi_3 = 1$ phase, C_b is charged to V_r and C_a discharged. In the next $\phi_1 = \phi_2 = \phi_3 = 0$ phase, two capacitors are connected in parallel, to produce the output voltage V_{o2} :

$$V_{o2} = \frac{C_b}{C_a + C_b} V_r. \quad (5)$$

In this $SH_2=1$ phase, S/H2 samples V_{o2} . Taking the difference between V_{o1} and V_{o2} , we have

$$V_{o,diff} = V_{o1} - V_{o2} = \frac{C_a - C_b}{C_a + C_b} V_r = x V_r. \quad (6)$$

The expression (6) holds true of any differential capacitance transducer with x being the measurand.

The main error sources involved in the interface are clock feedthrough from switches, the offset voltage, the gain error of the UGB, and the parasitic capacitances at node ©. The effect of clock feedthrough can be reduced by modifying the switching sequence, as shown in Fig. 3. The delayed periods τ_1 and τ_2 , τ_1' and τ_2' exist between ϕ_3 and ϕ_1 and ϕ_3 , ϕ_2 and ϕ_1 and ϕ_2 , respectively. In the $\phi_1 = \phi_2 = \phi_3 = 1$ phase, switch S_4 is first turned off. The clock feedthrough charge from S_4 is then injected to C_b . Next, switch S_1 is turned off, to inject the clock feedthrough charge to C_a . The clock feedthrough charges stored in C_a

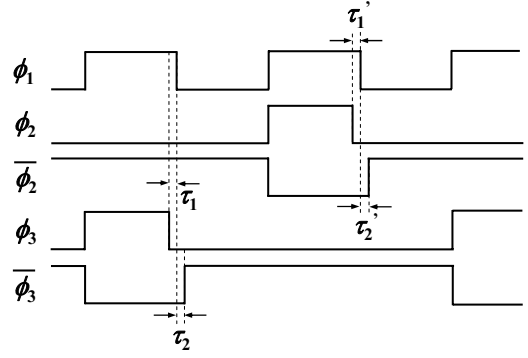


Fig. 3. Modified switching sequence.

and C_b are opposite in polarity but equal in magnitude if S_1 and S_4 consist of matched MOS transistors are turned off quickly [11]. Switch S_5 is turned on finally. In the next $\phi_1 = \phi_2 = \phi_3 = 0$ phase, these clock feedthrough charges are cancelled and have no effect on the voltage V_{o1} . The same operation is repeated for V_{o2} .

The offset voltages of the UGB are included in both V_{o1} and V_{o2} . Taking their difference in (6), they are cancelled. The gain error of the UGB causes that of the interface but dose not nonlinear error.

Let the parasitic capacitance at node ©, which include the finite input capacitance of the UGB be C'_{PC} . Then (6) is modified as follows,

$$V'_{o,diff} = \frac{C_a - C_b}{C_a + C_b + C'_{PC}} V_r \quad (7)$$

The parasitic capacitance at node © causes the gain error but dose not nonlinear error.

3. Performance simulated by HSPICE

Performances expected from CMOS realization are simulated by HSPICE with 0.35 μm n-well CMOS process parameters. CMOS switches with the aspect ratio $W/L_{PMOS} = 13.0\mu\text{m}/0.9\mu\text{m}$, $W/L_{NMOS} = 4.0\mu\text{m}/0.9\mu\text{m}$ are designed for implementation of the interface. Fig. 4 shows simulated performance of the interface using these switches and an ideal UGB. The total capacitor being 10 pF were used in place of a transducer. The power supply voltage V_{DD} is 3.3V. The clock frequency is 50 kHz. The reference voltage V_r is 1 V. The output voltage, $V_{o,diff}$, plotted in Fig. 4 (a) is proportional to the difference-to-sum ratio of two capacitors, confirming the ratiometric operation given by (6). Fig. 4 (b) shows deviations from the ideal values as the error voltage V_{error} . It can be seen that the error voltage, which is about 3.5 mV in a conventional interface [10], is reduced to small level in the proposed one. Modifying the switching sequence, it can be smaller.

A wide-swing CMOS UGB consisting of differential stage followed by a rail-to-rail output stage is designed for low voltage and low power operation [12]. The simulated dc gain is typically 78 dB and the dominant pole is located at 200 Hz. Performances of the interface using this UGB

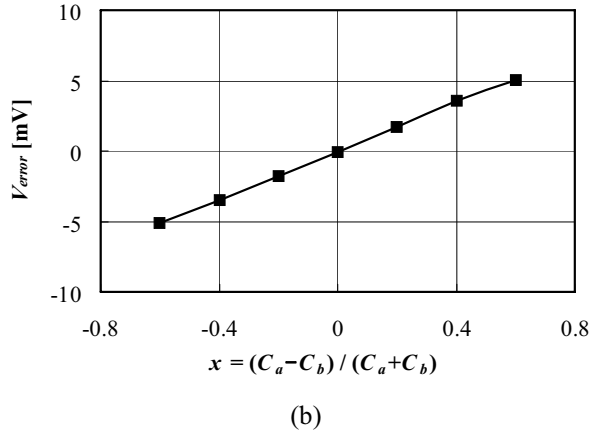
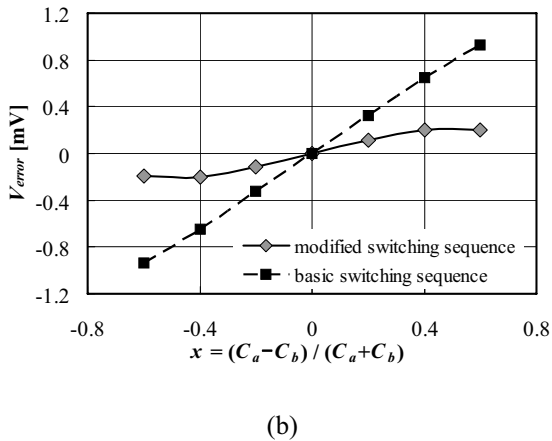
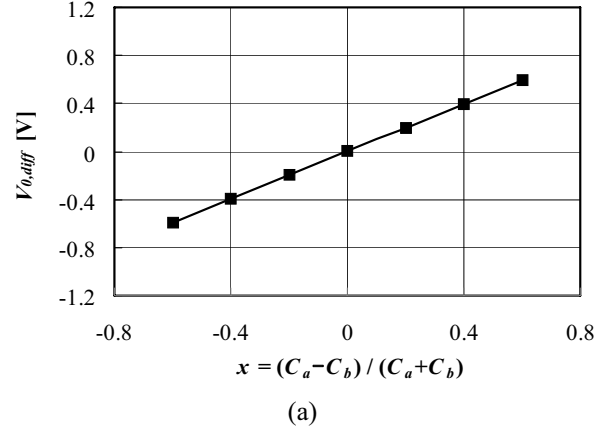
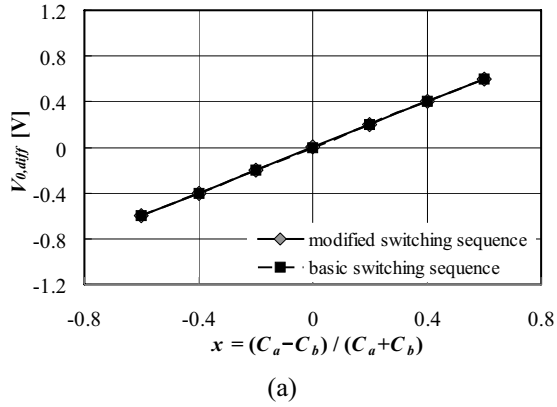


Fig. 4. Simulated performance of the interface using an ideal UGB: Differential output voltage (a) and the deviation from the ideal value (b) as a function of capacitance difference-to-sum ratio.

instead of the ideal one are shown in Fig. 5. These results indicate that the nonideal performances of the UGB causes the errors, but most of them are gain errors. Fig. 5(c) shows the residual nonlinear error is less than $\pm 0.2\text{mV}$. These results indicate that 0.1% resolution is achievable with the proposed interface, encouraging its CMOS realization.

4. Performance of Prototype Interface

A breadboarded interface using a OPA2340 op-amp and ADG612 switches, pairs of capacitors with the total capacitor C_o being 1000 pF, in place of a transducer, is used for experiments. The power supply voltage V_{DD} is 4 V. The clock frequency is 50 kHz. The reference voltage V_r is 2 V.

Typical measurement results are shown in Fig. 6. The output voltage plotted in Fig. 6 (a) is proportional to the difference-to-sum ratio of two capacitors, confirming the ratiometric operation given by (6). The nonlinear error, plotted in Fig. 6 (b), is of the order of a few mV.

5. Conclusions

A CMOS interface circuit based on a switched-capacitor sample/hold circuit using UGB of differential capacitance

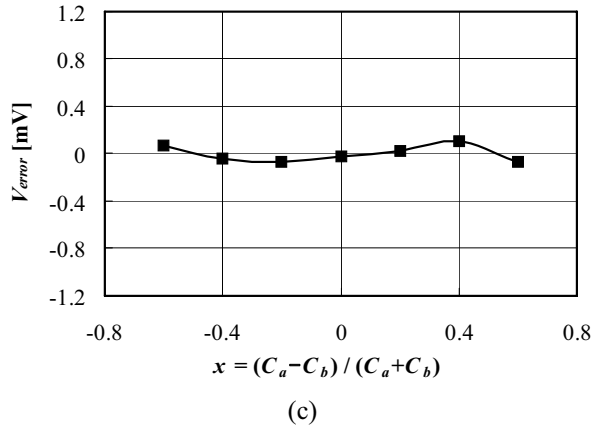
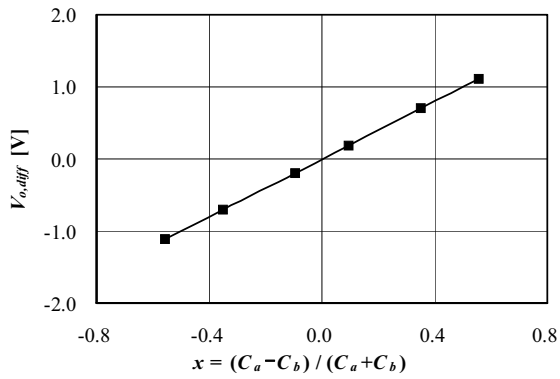
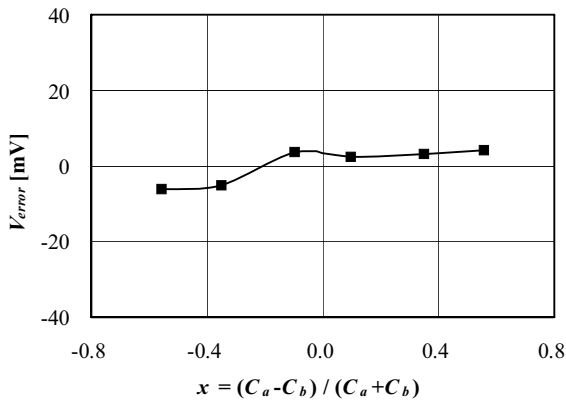


Fig. 5. Simulated performance of the interface using a CMOS UGB: Differential output voltage (a), the deviation from the ideal value (b), and the residual nonlinear error (c) as a function of capacitance difference-to-sum ratio.

transducers has been described which performs the ratiometric operation with the simple configuration. Simulated performances of the interface have shown that the ratiometric operation is sensitive to the nonideal performances of a UGB but they does not cause nonlinear error. Experimental results have also been given to confirm the principles of operation.



(a)



(b)

Fig. 6. Measured performance of the proposed interface: Differential output voltage (a) and the deviation from the ideal value (b) as a function of capacitance difference-to-sum ratio.

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