Autonomous Neuromorphic System with Four-Terminal Si-Based Synaptic Devices

Jungjin Park[1], Hyungjin Kim[1], Min-Woo Kwon[1], Sungmin Hwang[1] and Byung-Gook Park[1]
[1]Inter-university Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering,
Seoul National University, Seoul 151-744, Korea
E-mail: sharpjin@snu.ac.kr

Abstract: We have developed an autonomous neuromorphic system that can work with four-terminal Si-based synaptic devices. The symmetrical current mirrors connected to the n-channel synaptic devices constitute the synaptic connection and integration parts to express the excitation and the inhibition mechanism of neurons. The number and the weight of the synaptic devices affect the amount of the current flowing into the capacitor. The double-stage inverters controlling delay time and the NMOS with large threshold voltage (V_T) constitute the action-potential generation part. The generated action-potential is transmitted to the next neuron and simultaneously returned to the back gate of the synaptic device for expression of spike-timing-dependent plasticity.

Keywords— **Neuromorphic, Neuron Circuit, Synaptic Device, Action-Potential, Spike-timing-Dependent Plasticity (STDP)**

1. Introduction

As the conventional electronic system originated from Von Neumann's architecture has faced with fundamental physical limit and revealed the weakness in terms of cost and efficiency [1]-[4], we feel the need to introduce a new paradigm of information processing. As an alternative to the conventional system, the neuromorphic system inspired by human neural network has been developed recently. Reflecting the pros and cons of recent researches and considering space and power consumption, we proposed the neuromorphic system trying to emulate the neuron's mechanism with a small number of MOSFETs and introduced the Si-based synaptic device implementing the excitation and inhibition operation of the biological neuron. As we use 4-terminal Si-based synapses and connect them to the neuron circuit without the additional switch or logic operation, the proposed neuromorphic system can autonomously emulate the neuron's mechanism with minimum power dissipation.

2. Experimental Results

We designed the neuromorphic system as shown in Fig. 1. The neuron circuit is constructed by a total of 12 MOSFETs and 3 capacitors, except for synaptic devices, and consists of synaptic integration part and action-potential generation part. The integration part integrates and transmits the signal from pre- to post-neurons. The integration part is also divided into the excitation part and the inhibition part. The excitation part generates the current in the direction of increasing the capacitor voltage and the inhibition part generates the current in the reverse direction to the excitation part. The output pulse of the generation part is

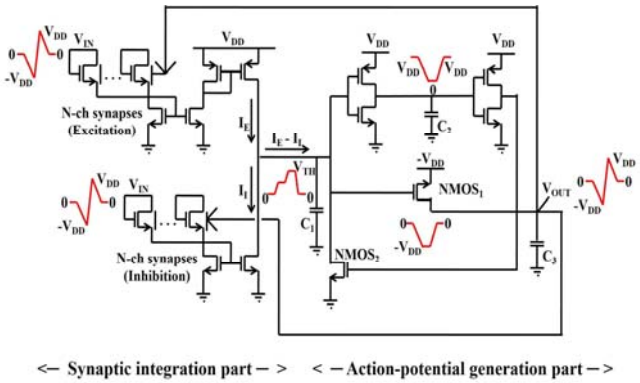

Fig. 1. Autonomous Neuromorphic System.

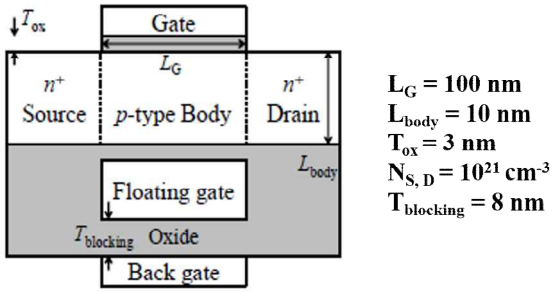

Fig. 2. Si-based floating-body synaptic transistor.

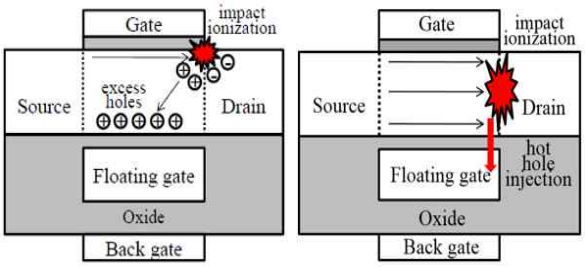

Fig. 3. Short-term to long-term transition in SFST.

fed back to the back gate of the synaptic device for the expression of spike-timing-dependent plasticity (STDP).

We used the Si-based floating-body synaptic transistor (SFST) [5, 6] in Fig. 2 that has short-term and long-term memory. Once the n-channel SFST is appropriately biased (e.g., V_G = V_{DS} = 2 V, V_{BG} = -2 V), excess holes are generated by impact ionization near the top gate and increase the potential of the body region to accelerate the impact ionization. This positive feedback process lowers the energy barrier between the source and the body and the threshold voltage (V_T) of the SFST. At the point when the source-body junction is forward biased due to the excess holes, the impact ionization occurs near the back channel and the generated hot holes start to enter the floating gate as shown in Fig. 3. Then, the decrease of the V_T becomes

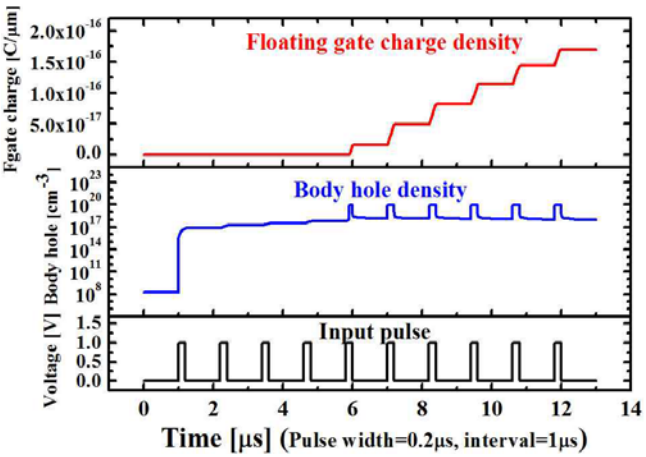

Fig. 4. Transient tendency of hole concentration in body and floating gate in SFST.

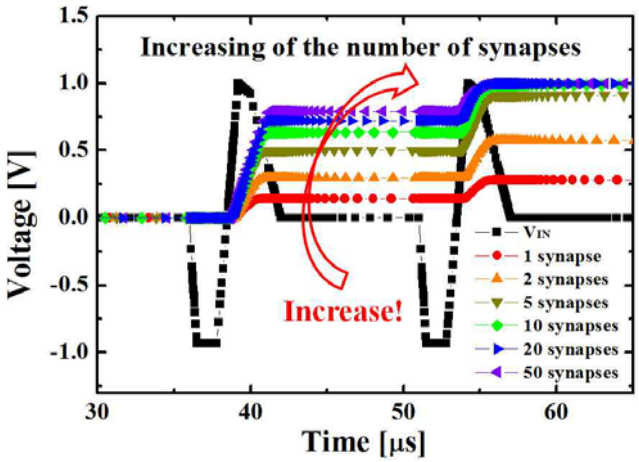

Fig. 6. Increase of V_{C1} in time domain with respect to the number of synaptic devices.

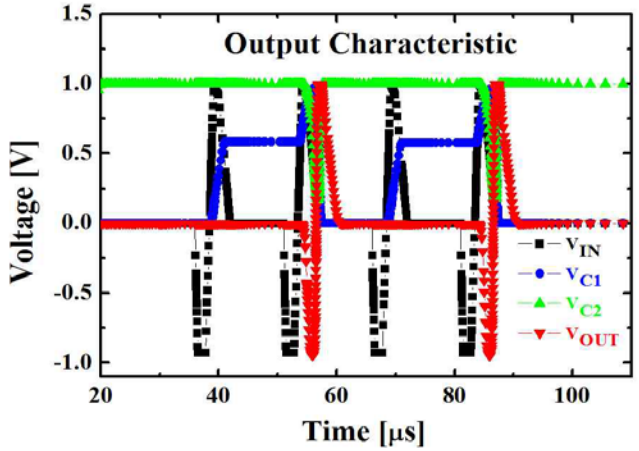

Fig. 5. Operation characteristic of neuron circuit.

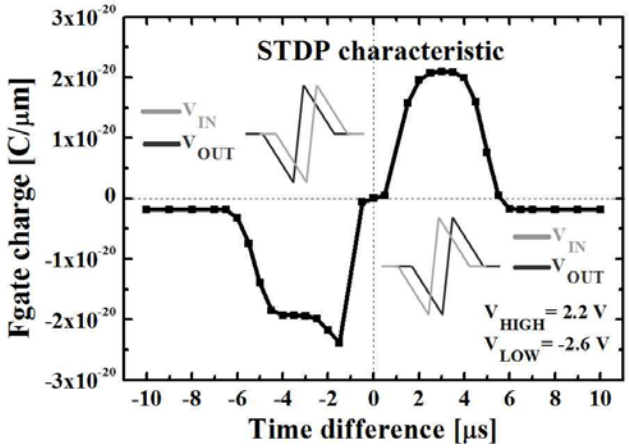

Fig. 7. Spike-timing-dependent-plasticity (STDP) curve from the system.

permanent and the above process corresponds to the short term to long-term transition of the memory. Fig. 4 shows the transient tendency of the hole accumulation in the body from the impact-ionization near the drain and the hole injection into the floating gate. In order to observe the motion of the holes dramatically, we applied the bias voltages to the synaptic device such as $V_G = V_{DS} = 1$ V, $V_{BG} = -2.5$ V and set the pulse width and the interval to 0.2 μs and 1 μs, respectively. As shown in Fig. 4, the triggering point that the holes are explosively generated and injected into the floating gate takes place when the 5th pulse is applied to the device.

Fig. 5 shows the operation characteristics of the proposed system. The action-potential generation part in the proposed system creates an action-potential when the node voltage of capacitor C_1 (V_{C1}) exceeds the threshold value. When the generation part turns on, the negative output of the $NMOS_1$ appears first and the positive delayed output from the double-stage inverters appears later to switch on the $NMOS_2$. Finally, the $NMOS_2$ discharges the V_{C1} and the system returns to its initial state. Fig. 6 shows that the firing of the system depends on the number of the synaptic device. Fig. 7 shows the experimental results of implementing STDP in the system. As the output pulse is generated immediately after the input pulse is applied, more hot holes enter into the floating gate of the SFST and stronger long-term potentiation is formed. In case that there is no causation between the input and the output pulses, the output pulse may fire before the input pulse of the synapse. Therefore, more electrons enter into the floating gate and stronger depression is formed.

Fig. 8 shows the simple diagram that the total of three neuron is connected in series and the output of pre-neuron is directly transmitted to the input of post-neuron. The additional terminal which takes inhibitory signal inhibiting the firing of the neuron is set up to each neuron and the initial input signal of 1st neuron is square pulse. Fig. 9 explains the way how the output of the pre-neuron affects the operation of the post-neuron. Fig. 9 (a) shows the case that any signal is not applied to the inhibitory terminal. When one input square pulse is applied to the 1st neuron, the 1st neuron fires and the output of the 1st neuron becomes the input of 2nd neuron. The number and the weight of the synapse are adjusted for the neuron to fire when the input action-potential is applied twice. Therefore, the 2nd neuron fires when the input action-potential is applied twice and the 3rd neuron fires based on the same rule. Fig. 11 (b) shows the case that the inhibitory signal is applied only to the 2nd neuron. Because the inhibited 2nd neuron can't fire, the following neurons can't fire. Similarly, when the inhibitory signal is applied only to the 1st or 3rd neuron, the

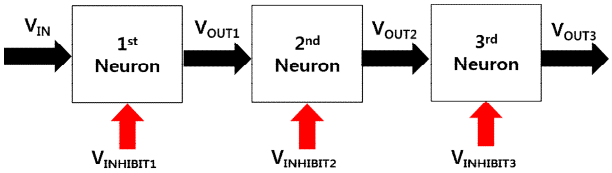

Fig. 8. The simple diagram that the total of three neuron is connected in series and the output of pre-neuron is directly transmitted to the input of post-neuron.

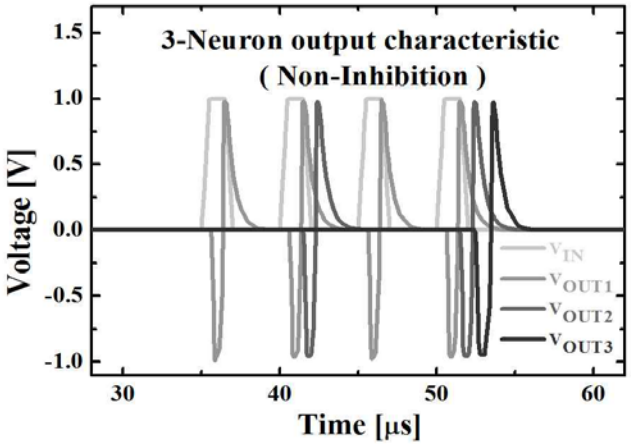

Fig. 9. Output characteristic of 3-Neurons connected in series. (a) When any signal is not applied to the inhibitory terminal, all neurons can fire in succession. When the inhibitory signal is applied only to the (b) 2nd neuron, the following neurons can' fire.

following neurons can't fire.

After verifying the operation of the neuron circuit and the synaptic device using simulation tool, we embodied the neuron circuit on printed circuit board (PCB). Fig. 10 (a) shows the layout of neuron circuit for fabricating the PCB and Fig. 10 (b) shows a scene for measuring the output characteristics of the fabricated PCB. We utilized a DC supply, pulse generator, oscilloscope for measurement of the PCB. As we applied square pulse train having a size of 2.2 V and a width of 3 μs to a single neuron, the output characteristic such as Fig. 11 (a) appears on the screen of

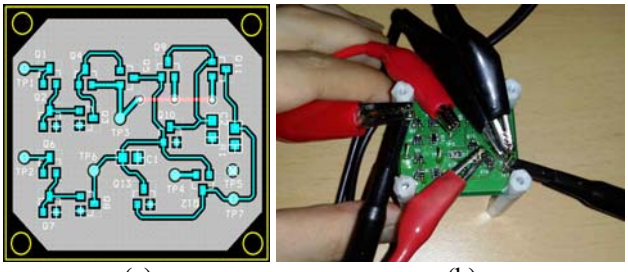

Fig. 10. (a) Layout of neuron circuit and (b) a scene for measurement of fabricated PCB.

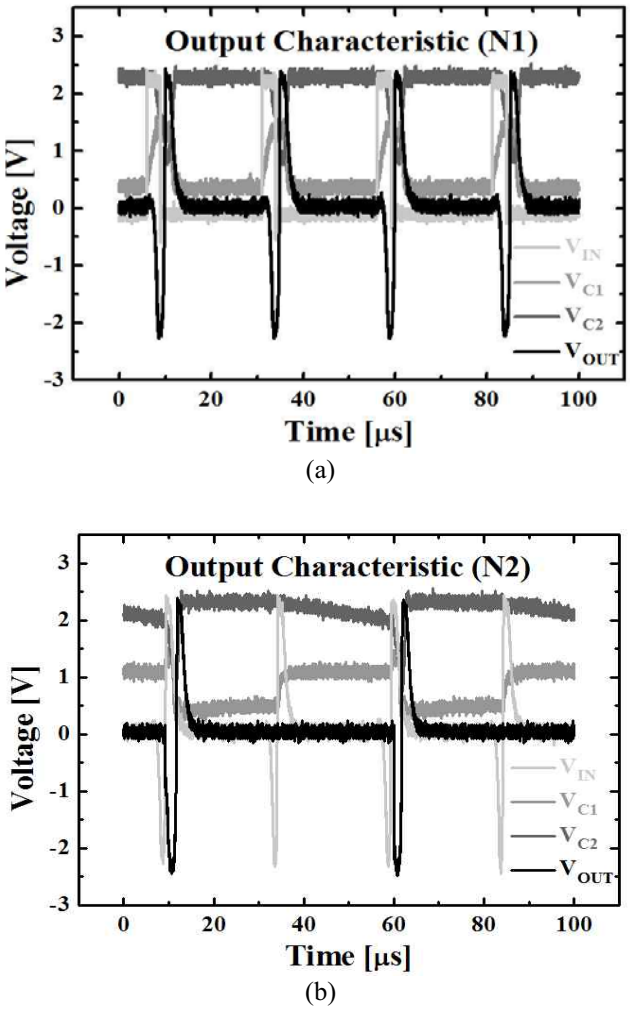

Fig. 11 (a) Operation characteristic of single neuron circuit and (b) a pair of neuron circuit connected in series

oscilloscope. Similar to the simulation results, as the square pulse is applied, enough charge for generation of action-potential is piled up to capacitor C_1 and the action potential having intended form is made. In case of Fig. 11 (b), we connected two neuron circuits in series and the output pulse of the 1st circuit was directly applied to the input of 2nd circuit. When the output pulse from the 1st neuron is applied twice to the input terminal of the 2nd neuron, the voltage of C_1 passes over the threshold point of the 2nd neuron circuit and action potential is generated.

3. Conclusion

We have developed an autonomous neuromorphic system based on Si-based synaptic transistors, current mirrors and double-stage inverters. We verified the operation characteristic of the system using simulation tool and PCB. Without additional switch and logic operation, it successfully implemented the important functions of the signal transmission in human neural network such as potentiation, depression, excitation, inhibition, and STDP. Since we implemented the neural mechanism with simple analog operation and the minimum number of transistors, the proposed neuromorphic system has possibility to be applied efficiently to the various neuromorphic applications with minimum power and space.

Acknowledgements

This work was supported by the Center for Integrated Smart Sensors funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012M3A6A6054186) and Samsung Electronics.

References

[1] R. Ananthanarayanan et al., “The cat is out of the bag: Cortical simulations with 10^9 neurons, 10^{13} synapses”, in Proc. *IEEE/ACM Conf. High Perform. Netw. Comput.*, 2009, pp. 1–12.

[2] S. Yu et al., “An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation”, *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2729–2737, Aug. 2011.

[3] K. D. Cantley et al., “Hebbian learning in spiking neural networks with nanocrystalline Silicon TFTs and memristive synapses”, *IEEE Trans. Nanotechnology,* vol. 10, no. 5, pp. 1066–1073, Sep. 2011.

[4] C. Zamarreño-Ramos et al., “On spike-timing-dependent-plasticity, memristive devices, and building a self-learning visual cortex”, *Front. Neurosci*, vol. 5, art. 16, Mar. 2011.

[5] H. Kim et al., “Silicon-based floating-body synaptic transistor,*” Int. Conf. on Solid State Devices and Materials*, pp. 322-323, Sep. 2012.

[6] H. Kim et al., “Silicon-Based floating-body synaptic transistor with frequency-dependent short- and long-term memories,” *IEEE Electron Device Letters*, vol. 37, no. 3, pp. 249-252, Mar. 2016.

[7] Y. Ota et al., “Analog implementation of pulse-coupled neural networks”, *IEEE Trans. Neural Netw*., vol. 10, no. 3, pp. 539-544. May. 1999

[8] C. Lu et al., "Circuit design of an adjustable neuron activation function and its derivative," *Electronics Letters,* vol. 36, no. 6, pp. 553-555, Mar. 2000.

[9] M. Boegerhausen et al., "Modeling short-term synaptic depression in silicon," *Neural Comput.,* vol. 15, no.2, pp. 331-348, Feb. 2003.

[10] T. Asai et al., "A subthreshold MOS neuron circuit based on the Volterra system," *IEEE Trans. Neural Netw.,* vol. 14, no. 5, pp. 1308-1312, Sep. 2003.

[11] G. Indiveri, E. Chicca, and R. Douglas, "A VLSI array of low-power spiking neurons and bistable synapses with spike-timing dependent plasticity," *IEEE Trans. Neural Netw.,* vol. 17, no.1, pp. 211-221, Jan. 2006.

[12] J. H. Wijekoon and P. Dudek, "Compact silicon neuron circuit with spiking and bursting behaviour," *Neural Netw.,* vol. 21, pp. 524-534, Mar. 2008.

[13] S. Ambrogio et al., "Spike-timing dependent plasticity in a transistor-selected resistive switching memory," *Nanotechnology,* vol. 24, no. 38, pp. 384012-384020, Sep. 2013.

[14] S. Yu et al., "A neuromorphic visual system using RRAM synaptic devices with Sub-pJ energy and tolerance to variability: Experimental characterization and large-scale modeling, in *IEDM Tech. Dig.,* 2012, pp. 239-242.

[15] S. Park et al., "RRAM-based synapse for neuromorphic system with pattern recognition function," in *IEDM Tech. Dig.,* 2012, pp. 231-234.

[16] K.-H. Kim et al., "A functional hybrid memristor crossbar-array/CMOS system for data storage and neuromorphic applications," *Nano letters,* vol. 12, pp. 389-395, Dec. 2011.

[17] M.-W. Kwon et al., "Integrate-and-Fire neuron circuit and synaptic device using floating body MOSFET with spike timing- dependent plasticity," *Journal of Semiconductor Technology and Science*, vol. 15, no. 6, pp. 658-663, Dec. 2015