Reconfigurable U-shape Tunnel FET

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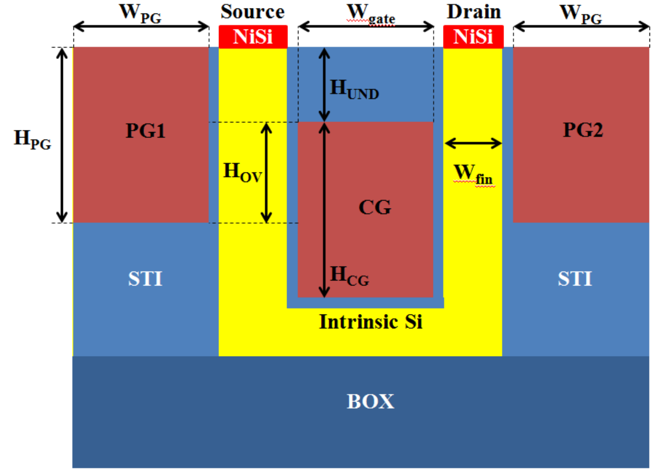
Abstract: In this paper, we propose and validate a novel design of dynamically reconfigurable tunnel field-effect transistor having a U-shape channel and three gates (two polarity gates and one control gate). The polarity gate acts on the side regions of the channel, swithcing the device polarity dynamically between *n* and *p*-type. Also, the conduction mechanism of proposed device is based on the tunnel FET operation that features low-leakage current, low power consumption, and scalable subthreshold swing (*SS*). To improve on-current drivablity and suppress short-channel effect, we propose a unique U-shape channel structure. The designed device provides ~30× higher on-current(I_{on}) and an average subthreshold swing of 41.8 mV/dec.

1. Introduction

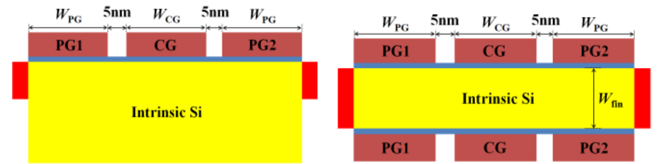
As we are moving toward a sub-20-nm CMOS technology regime, various new transistors are proposed to overcome conventional CMOS transistor limitations, such as short-channel effects (SCEs) and random dopant fluctuation (RDF). A Tunnel field-effect transistor (TFET) is the most promising candidate for a next-generation transistor device supplanting a standard MOSFET[1]. However, technical issues still remain for its commercialization such as poor on-current drivability due to its limited band-to-band tunneling (BTBT) through shallow inversion layer. Another problem with TFET is that the requirements of higher doping concentration and abrupt doping profile at juctions further detriment the SCEs and RDF.

Another limitation of CMOS transistors is a lack of flexibility related with circuit design. CMOS transistors are limited to static electrical fuctions that cannot be changed. The dynamically configurable devices is another new solution that can be reversely configured as *n* or *p*-type simply by the application of an electric signal[2]. In [3-4], configurable logic gates with polarity controlled silicon nanowire FETs have been dmonstrated. Also, TFET-based reconfigurable transistor have been proposed[5]. However, this device several inherent drawbacks originated from conventional TFET.

In this manuscript, we propose a reconfigurable U-shape tunnel FET (RUTFET). The characteristics of proposed device have been examined by technology computer-aided design (TCAD) simulation, Atlas Silvaco V5.19.20. Our designed device provides full flexibility by yiedling symmetric I_D-V_G characteristics, scalable *SS*, and high I_{on} owing to unique U-shape structure. These features make way for a simple and compact hardware platform that can be flexibly reconfigured during operation to perform different logic computations.



(a)



(b) (c)

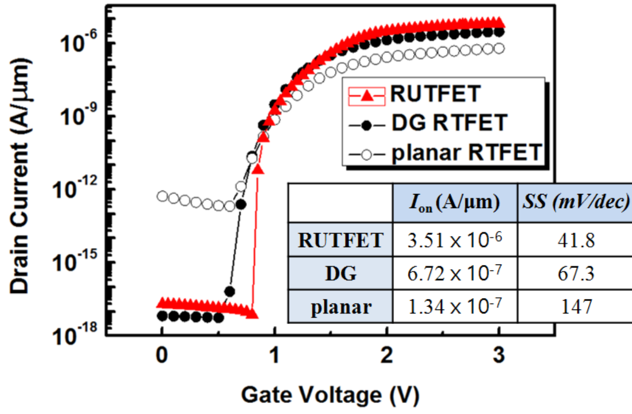
Fig. 1. Cross-sectional view of (a) RUTFET (b) planar-type reconfigurable TFET (c) DG-type reconfigurable TFET

Table 1. Parameters of the baseline of designed device

Parameter	Value
Metal gate work-function	4.6 eV
NiSi schottky barrier height	0.45 eV
EOT of gate dielectric	0.8 nm
Program gate (PG) width (W_{PG})	20 nm
Program gate (CG) width (W_{gate})	20 nm
Program gate (PG) height (H_{PG})	50 nm
Program gate (CG) height (H_{CG})	50 nm
Height of overlap between PG and CG in RUTFET(H_{OV})	20 nm
Silicon fin width (W_{fin})	6 nm
Height of underlap between PG and CG in RUTFET(H_{UND})	30nm

2. Device Structure and Simulation Results

The structures of RUTFET and conventional reconfigurable TFETs (planar type and double-gate type) are depicted in Fig. 1. In the RUTFET, dopingless Si channel based on SOI(Silicon-On-Insulator) structure is used. And, the formation of source and drain is achieved with the application of appropriate bias at polarity gates (PGs)



	I_{on} (A/μm)	SS (mV/dec)
RUTFET	3.51 x 10^{-6}	41.8
DG	6.72 x 10^{-7}	67.3
planar	1.34 x 10^{-7}	147

Fig. 2. Transfer characteristics of RUTFET and conventional reconfigurable TFETs. (Bias condition of RUTFET : PG1= -1.2 V, PG2=1.2 V, Drain=1 V)

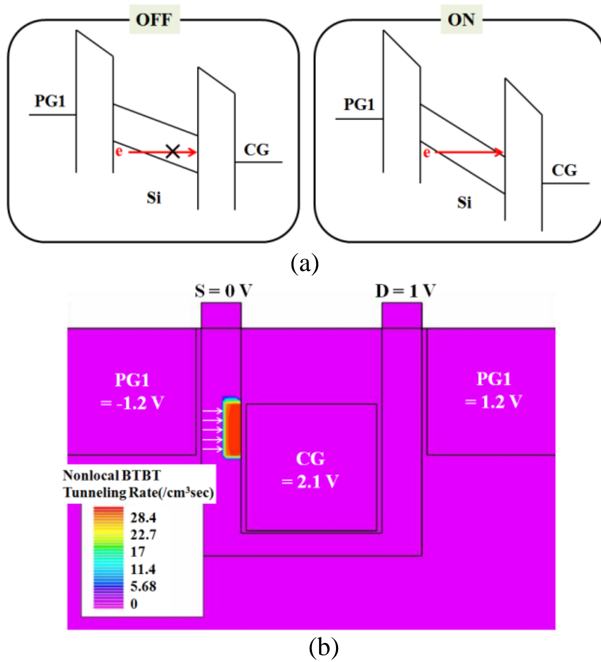


Fig. 3. (a) Energy band diagram along with overlap region from PG1 to CG in n-type RUTFET (b) two-dimensional contour plot of electron BTBT rate for n-type RUTFET.

(i.e., electrically doped). As a conseqeunce, the device becomes dynamically configurable to switch between *n*- and *p*-type TFETs. Also, the device has a U- shape channel structure that can make following advantages.

First, the recessed-channel structure is very heplful to address SCE with the help of increasd physical channel length. As a result, RUTFET can solve the SS degradation by a drain-induced barrier thinning (DIBT) [5].

Second, a large CG-to-PG overlap region can increase band-to-band tunneling (BTBT) juction area. As a result, the RUTFET can increase the I_{on}.

The conventional reconfigurable TFETs and the proposed RUTFET are simulated using a TCAD device simulator, Atlas Silvaco. The nonlocal band-to-band tunneling (BTBT) model based on Wentzel-Kramer-Brillouin (WKB) is enabled in order to calculate the tunneling probability using an electron-hole wave vector throughout the tunneling path [6].

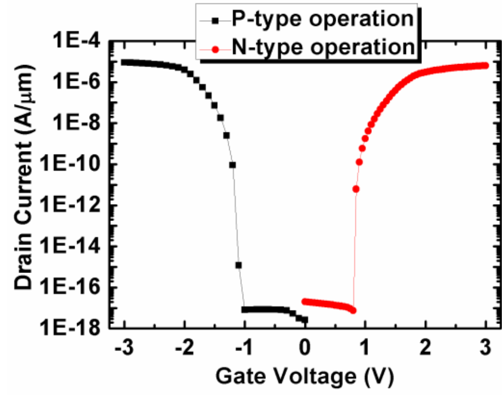


Fig. 4. Dynamic reconfigurable characteristics of *n* and *p*-type operation. (p-type operation condition : PG1= 2 V, PG2= -2 V, Drain= -1 V)

The trap-assisted tunneling model given by Schenk is also enabled. Since RUTFET use NiSi contacts at the drain and the source, we enable the universal Schottky tunneling model.

Key parameters of devices for simulation are summarized in Table 1. Metal work function for PGs and CG is 4.6 eV. And, source and drain contact made up of nickel silicide (NiSi) with a barrier height of 0.45 eV.

2.1 Device Transfer Characteristics

To demonstrate significant improvement of RUTFET, the basic transfer characteristic is compared with other reconfigurable TFETs as shown in Fig. 2.

A turn-on voltage ($V_{turn\text{-}on}$) is defined as gate voltage when drain current (I_D) is 10^{-12}A/μm. A *SS* indicates a reciprocal of mean ratio of change in the log(I_D)-V_G curve when I_D increases from 10^{-12} A/μm to 10^{-7} A/μm. Lastly, I_{on} is extracted for V_g=$V_{turn\text{-}on}$+1.0 V. As indicated in Fig.2, the *SS* of RUTFET is far smaller those of conventional reconfigurable TFETs. In the case of RUTFET, maximum barrier width (W_t) is fixed by silicon fin width (W_{fin}). As illustrated in Fig. 3(a), the BTBT is not occured until the valence band edge (E_V) on the PG1 side is aligned with the conduction band edge (E_C) on the CG side. As a result, RUTFET has higher BTBT probability at $V_{turn\text{-}on,}$ resulting in more abrupt on/off transistion than conventional reconfigurable TFETs(DG RTFET and planar RTET).

In addition, RUTFET shows ~30 x higher I_{on} than planr reconfigurabl TFET. The BTBT of planar TFET occurs through the thin inversion laer (~2 nm). On the other hand, in the case of RUTFET, the tunneling occurs through the vertical channel at the PG1/CG overwrapped regions as shown in Fig. 3(b). Furthermore, we can modulate I_{on} without additional area size by scaling the height of vertical overwrapped region(H_{ov}).

The proposed RUTFET features higher on-current and lower subthreshold swing than previous reconfigurable TFETs. Therefore, RUTET may provide a promising solution to next-generation transistor technology.

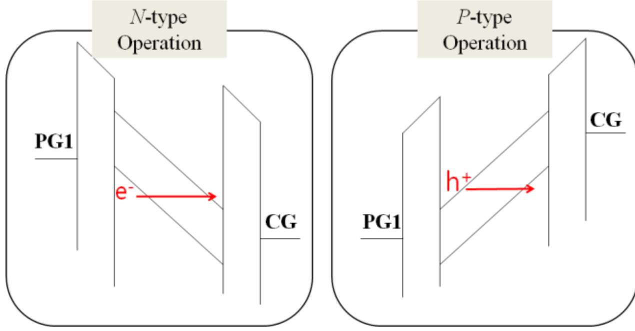


Fig. 5. Schematic band diagram and each tunneling mechanism of *n*- and *p*- type operation.

2.2 Reconfigurable Operation

To realize electrical n+ or p+ region in the proposed RUTFET, appropriate biases need to apply across PGs. A positive bias create n+ region, and a negative bias can create p+ region. As a result, the polarity of the same transistor can be seleced by simply applying a program potential at PG electrodes.

To guarantee the dynamic configurability and symmetric transfer characterisitics, we reversed the bias across PGs that represent p-type RUTFET and observed the I_D-V_G characteristics, as indicated in Fig. 4. Different voltages are applied on *n*- and *p*- type PGs in order to obtain symmetric drain current level.

The tunneling probability based on the nonlocal BTBT model with WKB approximation use the following equation

$$T(E) = \exp\left(-2\int_{x_{start}}^{x_{end}} k(x)\right) \quad (1)$$

where x_{start} is the start point of the tunneling paths, x_{end} is the end point of the tunneling parth, and k(x) is the evanescent wavevector at point x. The wavevector k(x) can be described as

$$k(x) = \frac{k_e k_h}{\sqrt{k_e^2 + k_h^2}}. \quad (2)$$

The each wavevector is given by the following equation:

$$k_e(x) = \frac{1}{i\hbar}\sqrt{2m_0 m_e(x)(E - E_c(x))} \quad (3)$$

$$k_h(x) = \frac{1}{i\hbar}\sqrt{2m_0 m_h(x)(E - E_c(x))} \quad (4)$$

where m_e is the electron effective mass, m_h is the hole efective mass, and m_0 is the electron rest mass.

In case of p-type operation, a hole has a larger effective mass than that of electron, which leads to smaller BTBT rate. Consequently, we should apply higher voltage on *p*-type PGs to make similar BTBT rate with *n*-type operation.

As shown in Fig. 4, the symmetric I_D-V_G characteristics, high on-current drivability and steep *SS* of the proposed device make it a suitable candidate for dynamically configurability with high performance. This implies that the potential to change the configuration of each transistor within the circuit enalbes the reconfiguration of logic circuit in a fine grain manner. Specific logic functions can be dynamically altered during user operation. As a consequence, the main advantage of the reconfigurable operation of RUTFET is that additional logic fuctions can be provided with the same number of transistors compared to standard CMOS logic.

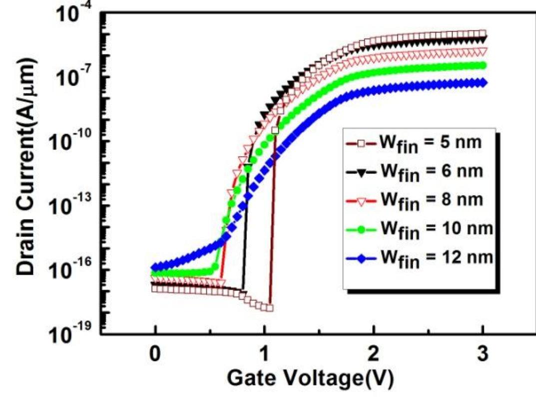


Fig. 6. Transfer curves with the variation of $W_{\rm fin}$ ranging from 5 to 12 nm.

Fig. 5 presents a conceptual band diagram showing the tunneling mechanism in RUTFET at diference PG1 and CG biases. A negative PG1 bias and a positve CG bias allows electron to create a current through the n-channel. On the other hand, a positive PG1 bias and a negative CG bias make hole tunneling to make *p*-type operation.

2.3 Device Characteristics Study

Fig. 6 shows the transfer characteristic with various $W_{\rm fin}$ (intrinsic silicon width between CG and PGs). The silicon fin width($W_{\rm fin}$) means the tunneling distance from $x_{\rm start}$ to $x_{\rm end}$. It means that $W_{\rm t}$ is determined by $W_{\rm fin}$ which is not controlled by electrical bias but by fabrication process.

As shown if Fig. 6, *SS* increases as $W_{\rm fin}$ increases from 5 nm to 12 nm. When $W_{\rm fin}$ is large, even if the $E_{\rm V}$ of the PG1-side silicon channel region is aligned with the $E_{\rm C}$ of the CG-side silicon channel region, $W_{\rm t}$ is still large. It leads to high off-current and large *SS*. Furthermore, off-current increase lowers $V_{\rm turn\text{-}on}$ as shon in Fig. 6. On the other hand, as $W_{\rm fin}$ becomes smaller, $W_{\rm t}$ becomes smaller as long as the $E_{\rm V}$ of the PG1-side silicon channel region is aligned with the $E_{\rm C}$ of the CG-side silicon channel region. At the same time, it becomes more difficult to make the $E_{\rm V}$ of the PG1-side silicon channel region aligned with the $E_{\rm C}$ of the CG-side silicon channel region due to small $W_{\rm fin}$. It results in small *SS* and high $V_{\rm turn\text{-}on}$.

From now on, the tendency of $W_{\rm fin}$ from the viewpoint of $I_{\rm on}$. The electric field to make BTBT current is governed by the following equation :

$$\text{Electricfield} \approx \frac{V_{\rm PG1} - V_{\rm CG}}{W_{\rm fin}} \quad (5)$$

Consequently, as $W_{\rm fin}$ becomes smaller, electric field becomes larger, which leads to higher BTBT rate. As shown in Fig. 6, $I_{\rm on}$ increases as $W_{\rm fin}$ decreases from 12 nm to 5 nm.

Therefore, when we design the specific physical parmaeter of RUTFET, a thin silicon fin width is desirable.

3. Conclusion

A novel reconfigurable U-shape TFET(RUTFET) has been proposed for dynamically configurable applications. The p^+ and n^+ are induced on a intrinsic silicon channel via PG biasing. A RUTFET features band-to-band tunneling direction perpendicular to the channel. Because the W_t and tunneling juction cross-sectional area are determined by W_{fin} and overlap between PG and CG (H_{OV}), respectively, RUTFET show better performance than previous ones in terms of *SS* and I_{on}. The superiority of RUTFET have been demonstrated using 2-D TCAD simulations. Therefore, it is expected that a reconfigurable U-shaped TFET will be the most promising candidate for a next-generation electron devices.

Acknowledgement

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