A Subthreshold Ultra-Low Power Low-Voltage High Resolution DCO using Al Pad metal Layers for BLE Application in 55 nm Technology

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Abstract: This paper presents the design and implementation of an ultra-low power Digitally Controlled Oscillator (DCO) for Bluetooth Low-Energy (BLE) applications which has wide tuning range about 4.2 GHz ~ 6.1 GHz. The device consists of MOSFET circuits operating in the sub-threshold region and the power dissipation is reduced by sub-threshold design. High frequency resolution is achieved by using the fine tuning bank and the Delta-Sigma Modulator (DSM). A very small capacitance, about 16.22 aF through customized lateral MOM capacitor is utilized for attaining small switchable capacitance in fine tuning bank. To eliminate routing metals' parasitic inductance, a ultra-wide Aluminium (Al) pad metal layers are incorporated as a supper conductor. The proposed DCO is designed using CMOS 55 nm process. The S-parameter based simulation results prove that the current consumption is 480 μA at center frequency of 4.88 GHz at 0.55 V supply voltage. Also, high frequency resolution of 4.8 kHz is achieved. The DCO phase noise is about -114.1 dBc/Hz at 1-MHz offset. The layout size is 250×470 μm^2.

Keywords-- **DCO, ADPLL, ultra-low-power, low phase noise**

1. Introduction

In recent years, with the advancement of the technology, design of low power devices such as Wireless Personal Area Network (WPAN), biomedical systems, and portable devices has received more attention. The WPAN applications have triggered the needs for low-cost and low-power phased-locked loops (PLLs) which also provide good performance. The All-digital PLLs (ADPLLs) are preferred over their analog counterparts in nanoscale CMOS technology due to their configurability, flexibility, small area and easy portability [1]. However, fractional spurs and insufficiently low power dissipation are main problems related to conventional divider TDC-based structures. The DCO is one of the sub-blocks in divider TDC-based ADPLL which consumes the major power of the system and it generates local frequency [1-4]. Therefore, Design of an ultra-low power DCO will decrease the power consumption of the system significantly.

In this paper, an ultra-low power DCO is presented for System on Chip (SoC) BLE applications. The BLE application requirements mostly correspond to a low-power design. The design of a digitally controlled LC oscillator is based on a series of specifications which is dictated by the ADPLL design. The tuning range, power consumption, frequency resolution and phase noise are among the most important specifications which determine the DCO and ADPLL performance. The coarse-fine architecture, three capacitor banks, are adopted with binary weighted unit cells for high resolution to satisfy channel spacing specification of BLE application. For the fine tuning stage, an ultra-small atto Farad integrated metal capacitor using capacitor between metal layers is designed which shows high linearity and good performance.

2. Proposed DCO Design and Implementation

The top block diagram of CMOS cross-coupled DCO is depicted in Fig. 1. The basic function of a DCO is to generate a periodic signal whose frequency is digitally controlled by a control word. There are several DCO topologies which can be used in an ADPLL. The LC oscillators are mostly used in transceiver designs. In DCO, the frequency is tuned by switched capacitor array and its minimum capacitance step limits frequency resolution.

The designed DCO has three capacitor banks namely MSB, LSB, and Fine tuning. These banks are designed with unit binary constructs to obtain linear frequency step. The configuration of unit switched capacitor cell for MSB & LSB banks is shown in Fig. 1. This unit cell is comprised of two capacitors, two blocking resistors, and a switch. In MSB/LSB capacitor banks, MOM capacitors are employed to increase Q-factor.

In advance deep submicron process, MIM capacitance does not be provided for reliability. In fine capacitor bank, the configuration of unitcell can be changed. Normally, the unit capacitance in fine tuning bank is about a few atto Farad. To obtain small switchable capacitance in fine tuning bank, customized lateral MOM capacitor is employed and its capacitance is about 16.22 aF. The location of gm-cell is also issues. There are trade-off between power consumption and frequency range. If gm-cell is located in end of capacitor banks, the DCO has large parasitic inductance when all switched are turned off. The parasitic inductances causes decrease of oscillation frequency.

However, the inductance helps to reduce current dispassion. Reversly, if gm-cell is located in the neck of inductor, gm-cell can degrade Q-factor of inductor and increase power dissipation. The location of gm-cell in proposed DCO is at the end of capacitor banks to reduce the power consumption. The MOS transistors of designed DCO optimally biased in subthreshold region (V_{GS}-$V_{TH} \approx 0.1V$) are utilized to provide enough transconductance for a given bias condition, resulting in reduction of the power dissipation of the DCO.

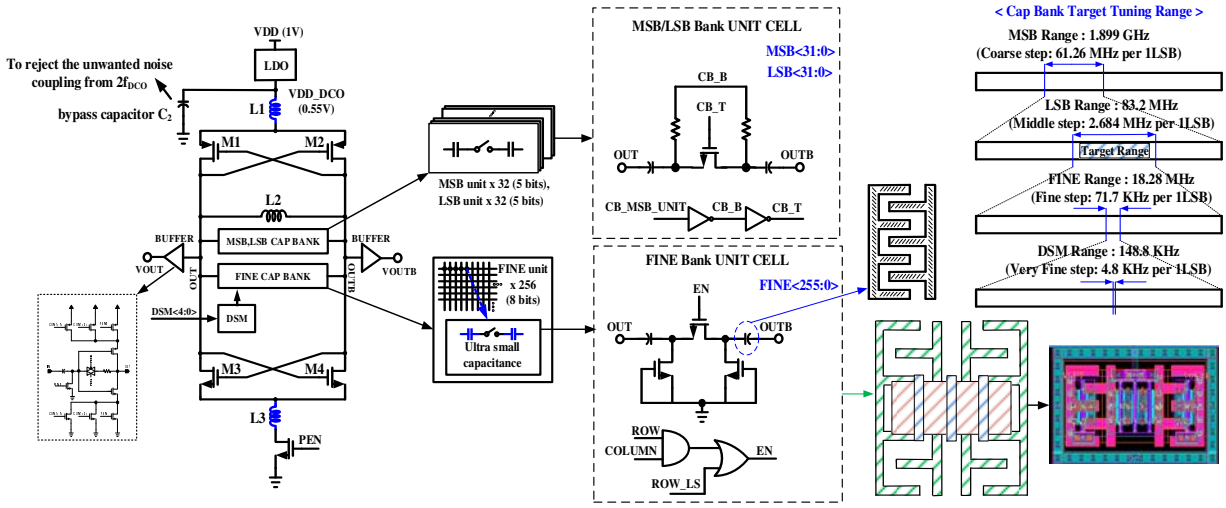

Figure 1. Complete schematic of proposed ultra-low power low-voltage DCO circuit

3. Post-layout Simulation Results

The designed DCO is post-layout simulated in 55 nm CMOS technology with power supply of 0.55 V and its oscillation frequency is 4.88 GHz. Results show that the designed DCO achieves 4.2 ~ 6.1 GHz frequency range. 1bit resolution of MSB, LSB, Fine cap banks, and DSM are 61 MHz, 2.6 MHz, 72 kHz, and 4.8 kHz respectively. The top-level DCO layout is shown in Fig. 2. The active area of the DCO is 0.1175 mm^2 which is mainly determined by the inductor. Figure 3 shows the output of the DCO obtained from the transient and periodic steady-state (PSS) analysis. The Phase noise and current consumption of the proposed DCO circuit are also shown in Fig. 3. A phase noise of about -114.1 dBc/Hz at 1 MHz offset from the operating frequency and current consumption of around 480 µA are achieved. The designed DCO has 32-MSB, 32-LSB, and 256-Fine capacitor unit. The DCO covers the frequency of 4.2 GHz ~ 6.1 GHz with the covered target frequency bands. Finally, the proposed DCO's performance and its comparison with existing state-of-the-art works are summarized in Table 1.

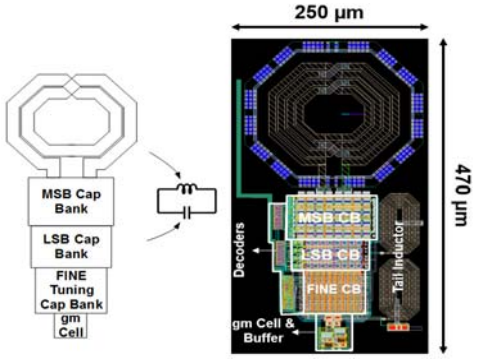

Figure 2. Chip Layout Pattern

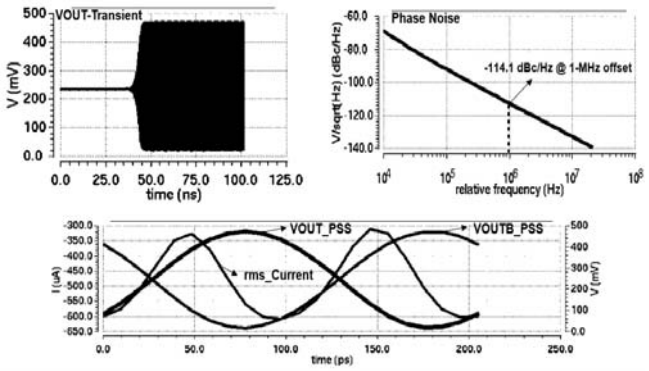

Figure 3. DCO post-layout simulation results

TABLE 1. Performance summary of the DCO and comparison

	This Work		*[1]*	*[2]*
Technology (nm-CMOS)	55		40	180
Oscillation Freq. (GHz)	4.88		2.44	3.2
1 bit Resolution	DSM	4.8 kHz	40 kHz	20 kHz
P. N. @ 1-MHz offset (dBc/Hz)	-114.1		-115.3	-114.42
Power Cons. (mW)	0.264		0.33	3.8

4. Conclusion

In this paper, a wide range, ultra-low power DCO with high linear step of capacitor banks is presented. The DCO is designed by sub-threshold for low-power and low-voltage operation. By using ultra-wide Al pad metal layers, the effective routing matels' parasitic inductance in proposed DCO can be eliminated. The DSM and The fine tuning bank which is designd by customized lateral MOM

capacitor are employed for high resolution. The power consumption is only 264 μW from 0.55 V supply voltage for the 4.88 GHz oscillation frequency.

Acknowledgment

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