A Low Power Coupling Shielded Digitally Controlled Oscillator (DCO)

Sang-Sun Yoo[1], Kang-Yoon Lee[2], and Hyung-Joun Yoo[1]
[1] The Department of Electrical Engineering,
Korea Advanced Institute of Science and Technology, Daejeon 3141, Korea
[2] The College of Information and Communication Engineering,
Sungkyunkwan University, Suwon 440-746, Korea
E-mail: [1]rapter@kaist.ac.kr, [2]klee@skku.edu

Abstract: This paper presents is a coupling shieled digitally controlled oscillator (DCO). The DCO has magnetic coupling shielding ring (CSR) which is designed with aluminum (Al) pad metal. This closed ring induces electromagnetic-force by Lenz's Low. As a results, designed DCO can be protected from the attack of power amplifier (PA) with strong magnetic field. The DCO was fabricated in 55-nm CMOS process. By using CSR, isolation between DCO and PA is increased about 11 dB witout degradations of performances.

Keywords—**Coupling shield, magnetic coupling, DCO, crosstalk,**

1. Introduction

Recently, the demands for low power and small size devices are rapidly increased with interests of bio-healthcare applications [1]. Since CMOS process has been shrank, the size of RFIC became much smaller and the distance between an inductor of PA and that of oscillator became also much closer. As a results, some coupling issues are newly appeared between PA and oscillator in small size of chip [2]. To reduce magnetic coupling between inductors, 8-shape inductor was reported previously [2][3]. 8-shape inductor can reduce magnetic coupling and increase isolation between inductors. However, its size is larger than normal spiral inductor and it can be only applied to 1-turn inductors. In low power applications, an LC-base oscillator requires multi-turn inductor with large inductance to reduce power consumption. Therefore, 8-shape inductor is not a candidate for low power RFIC.

In this paper, a low power coupling shielded DCO (CSDCO) is proposed. The DCO has coupling shield ring (CSR) for the cancelation of magnetic coupling from aggressor, e.g., power amplifier (PA). The CSR can increase isolation between PA and DCO about 11 dB without degradation of performances. The *FoM* of CSDCO is 190.2 dBc/Hz with 0.74-mW power consumption.

2. Coupling Shield Ring with Al Pad Metal

Figure 1 shows the 3D-diagram of proposed coupling shield ring. The CSR is designed with Al pad metal over a inductor of a DCO. The CSR can reduce mutual inductance between two inductors in Figure 1. When the current of the inductor is time-variant, the ring has induced current from magnetic field of the below inductor by Lenz's law. The induced current in CSR flows in opposite direction of the

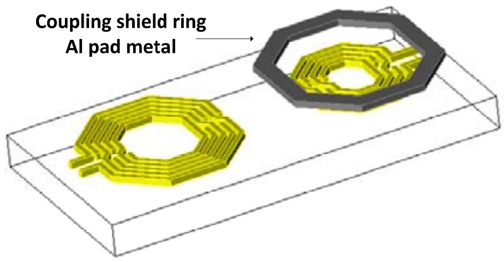

Figure 1. The 3D-graphic of proposed coupling shield ring (CSR)

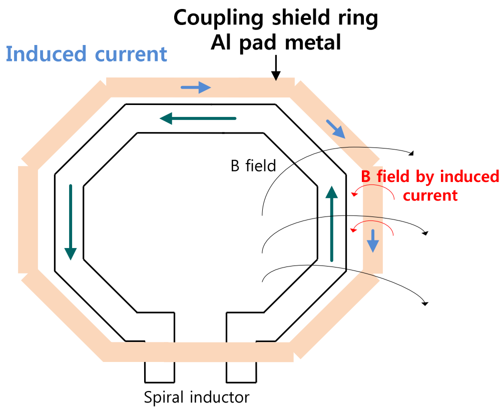

Figure 2. The cancelling of magnetic field by induced current

current in the inductor as shown in Figure 2. Then, induced current also makes magnetic field. Since the direction of induced magenic field by CSR is opposite to magnetic field by inductor, the integration of magnetic field is reduced at outside of inductor. Assuming that mutual inductances between PA and DCO is the same ($M_{21}=M_{12}$), magnetic field from PA to DCO is also decreased by induced current.

In a RFIC, there are two kinds of coupling. One is magnetic coupling and the other is sub-strate coupling. Since the role of CSR is the reduction of magnetic coupling by mutual inductance, CSR should be located over the inductor. If CSR is made by lower layer than that of inductor, there is no change of coupling ratios. For these reasons, CSR is designed with Al pad layer which is only upper layer than inductor layer. The Al pad layer is necessary and inevitable in CMOS RF process. It is used for crossing metal between ultra thick metals (UTM) in inductor layout. Therefore, there is no extra cost to employ Al pad layer for CSR. In addition, since CSR is located inside of a guard ring of inductor, the size of DCO is not increased.

3. Test DCO Design and Testbench for Verifying Reduction of Magnetic Coupling

A test DCO (TDCO) is designed with 55-nm CMOS process. To reduce power consumption, CMOS complimentary architecture is adopted with 0.8-V supply voltage. Designed TDCO has three capacitor banks such as MSB, LSB, and fine tuning capacitor bank. All capacitor banks are designed with unit weighted capacitor bank instead of binary weighted structure for linearity of frequency step. Although the size of unit weighted capacitor bank is slightly larger than that of binary capacitor bank by 5~10 %, it has many advantages in terms of linearity and flexibility for design [4]. Unit weighted capacitor bank can employ 24-capacitors which is not a binary number. The configurations of unit capacitor cell with switch in three-bank are shown in Figure 3.

To verify the enhancement of isolations, TDCO and coupling shield DCO (CSDCO) with an aggressor are implemented for comparing as shown in Figure 4. The schematic and layout of CSDCO are the same with TDCO except CSR. The distances to aggressor are also the same. For reconfigurability, a switch and DC blocking resistors are added in CSR as shown in Figure 5. When SW_{CSR} is turned off, this ring cannot effect mutual inductance due to open looped CSR. However, when SW_{CSR} is turned on, isolation between inductors may be increased because CSR become closed loop by a MOS switch. This close loop make induced current and magnetic field in opposite direction to those of inductor. The most important thing is that the isolation between inductors can be controlled by CSR with a switch.

4. Measurement Results

Figure 6 shows the output spectrum of CSDCO. When a switch of CSR (SW_{CSR}) is turned off, CSR cannot increase isolation because the loop is open. Then the coupling power from aggressor is about -55 dBm with -20-dBm input power where the largest tone in Figure 6 is oscillation spectrum of the CSDCO. Then isolation between aggressor and CSDCO is about 35 dB. Otherwise, when switch is turned on to make close looped CSR for high isolation, coupling signal power is decreased to -66 dBm with the same input power. It means that CSR increase the isolation about 11 dB. By this time, the oscillation frequency is shifted from 4.865 to 5.203 GHz by induced current of CSR. The CSR makes induced current and it degrades inductance of DCO from 1.55 to 1.36 nH (Δ = -0.19 nH). Figure 7 shows phase noise of CSDCO with CSR-ON mode. Measured phase noise is about -114.5 dBc/Hz @ 1 MHz. Table 1 shows the summary and comparison of the performances of DCOs. When a switch is turned on, isolation is increase about 11 dB whereas phase noise of CSDCO is only degraded about 0.5 dB. The overall performances of CSDCO are similar to those of TDCO which has no CSR in Figure 4. The overall performances of DCO can be represented by a figure-of-merit (*FoM*) as below [5]

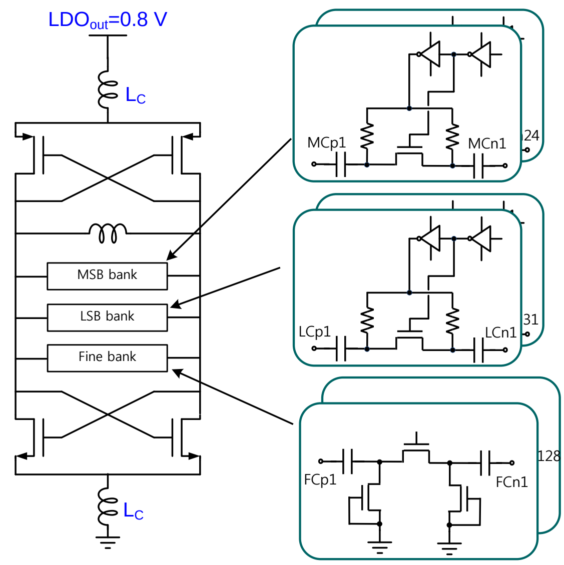

Figure 3. Schematic of designed DCO

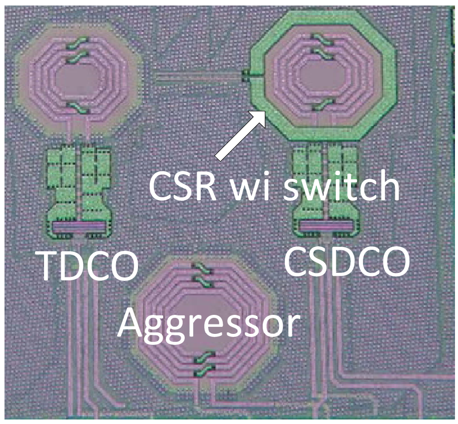

Figure 4. Die photo of TDCO and CSDCO

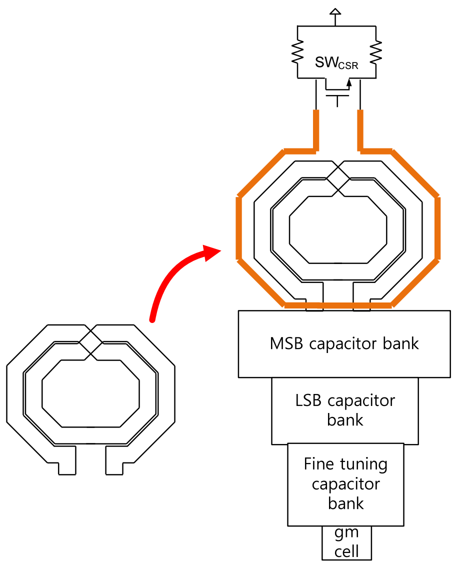

Figure 5. Advanced CSR with a MOS switch for reconfigurability

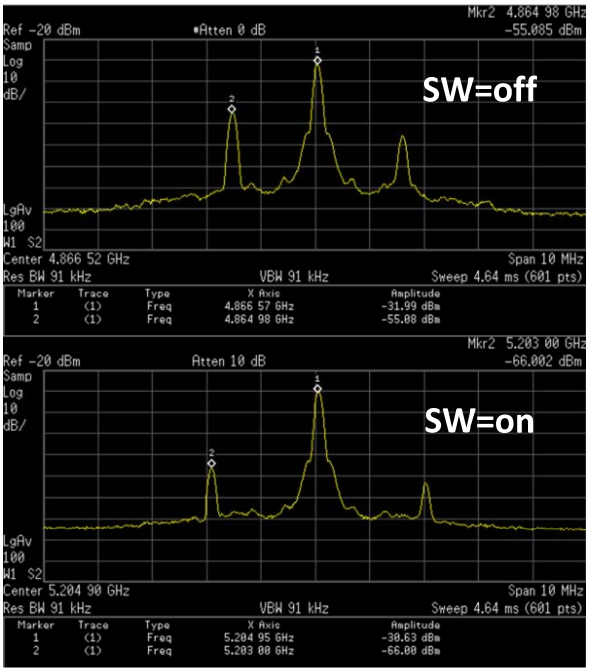

Figure 6. The output spectrum of CSDCO with aggressor according to on-off switch

$$FoM = -PN(f_{offset}) + 20\log\left(\frac{f_0}{f_{offset}}\right) - 10\log\left(\frac{P_{DC}}{1mW}\right) \quad (1)$$

The minimum *FoM* of designed DCO is 190.2 dBc/Hz, which is superior to that of previous works. The sizes of DCOs are the same about 220×360 μm^2.

5. Conclusions

Proposed CSR with a switch can increase the isolation of magnetic coupling about 11 dB without performance degradations. The fabricated CSDCO has a high *FoM* of 190.2 dBc/HZ with small power consumption about 0.74 mW. The CSR becomes more valuable in small size of RFIC.

Acknowledgment

This work was supported by "the Technology Innovation Program" (10052624, Development of SoC for Positioning Service using BLE v4.2 IP) funded By the Ministry of Trade, industry & Energy (MI, Korea)

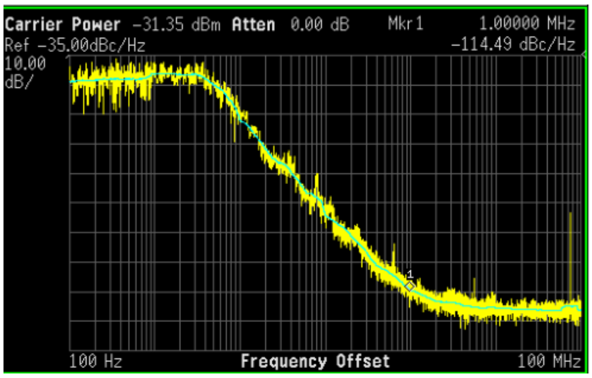

Figure 7. The phase noise of CSDCO when a switch of CSR is turned on.

Table 1. The summary of Performances

	TDCO	CSDCO (SW=0)	CSDCO (SW=1)
Frequency (GHz)	4.85	4.864	5.203
Supply voltage (V)	0.8	0.8	0.8
Current (mA)	0.85	0.86	0.92
Phase noise @ 1MHz (dBc/Hz)	-115.1	-115	-114.5
Isolation (dB)	-35	-34	-56
Area (μm^2)	220×360	220×360	220×360
FoM (dBc/Hz)	190.5	190.4	190.2

References

[1] B. G. Perumana, et. al., "A low-power fully monolithic subthreshold CMOS reveiver with ingrated LO generation for 2.4 GHz wireless PAN application," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, Oct. 2008.

[2] A. Poon, et. al., "Reduction of Inductive Crosstalk Using Quadrupole Inductors," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, June, 2009.

[3] P. Andreani, et. al., "A TX VCO for WCDMA/EDGE in 90 nm RF CMOS,"*IEEE J. Solid-State Circuits.* vol. 46, no. 7, July, 2011.

[4] A. Kavousian, D. K. Su, M. Hekmat, A. Shirvani, and B. A. Wooley, "A Digitally Modulated Polar CMOS Power Amplifier with a 20-MHz Channel Bandwidth," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2251 – 2258, Oct. 2008.

[5] L. Fanori and P. Andreani, "Highly efficient class-C CMOS VCOs, including a comparison with class-B VCOs," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1730–1740, Jul. 2013.