A Cost-Efficient Tuner Design for Digital TV Receiver

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Abstract

In this study, a single-chip is designed with MOS techniques for the digital TV tuner. The chip consists of the modules of low noise amplifier（LNA）, RF mixer, digital voltage control oscillator, and polyphase filter. The tuner is designed with the structure of a single conversion by mixing the Quadrature local signal with polyphase filter. The frequency band is designed from 530 MHz to 602 MHz for DTV channels in Taiwan. The gain of the entire tuner can be over 32 dBm, and the image rejection ratio（IRR）of the tuner is above 30 dBm. The local oscillator built-in digital-to-analog converter can be directly controlled by a digital code to select the TV channel. The silicon chip had been designed with a full-custom layout, where the chip size and core size is about 0.497 and 0.1095 mm^2, respectively, when implemented by TSMC 0.18μm CMOS process. The maximum power dissipation is about 136.7 *mW* when the chip works 3.3V.

KEYWORDS: DTV, polyphase, active filter, mixing, tuner, polyphase filter and LNA.

I. INTRODUCTION

A wireless RF communication systems had widely used for portable devices, such as cell-phone, TV receiver, and GPS and so on. For the portable device, the chip size and power dissipation is as small as possible [1-3]. The digital TV had been popular because of high quality and low noise. For TV broadcasting, the tuner is required to select the TV channel from the RF signal modulation. The main function of a tuner is to transform RF signal to IF (intermediate frequency) one for TV receiver. The single conversion requires a tracking filter that employs high Q inductance, which is hardly implemented in a silicon chip. The double conversion method is widely used to reject the image frequency for the cable TV systems. The architecture is shown in Fig. 1. The first is an up-conversion that modulates the video signal to the high frequency band. The frequency of the first local oscillator is 1220~2080MHz, and the TV band is from 48~860MHz. One can select the IF from the differential of mixing of local oscillator and TV signal. Due to harmonic frequency, the image signal would appears on spectrum.

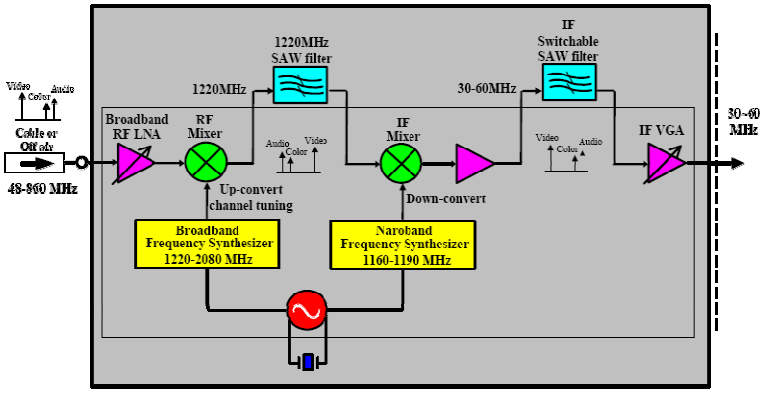

Fig. 1 The architecture of dual conversion with IF.

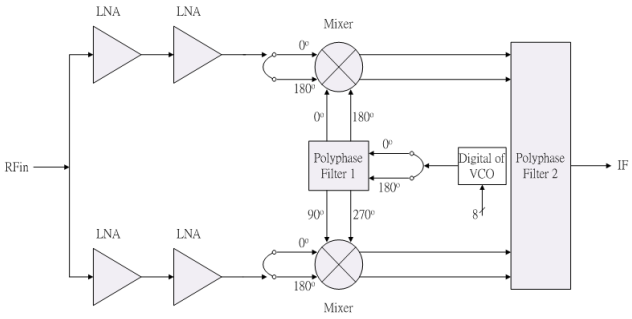

Figure 2 The architecture of the proposed DTV tuner.

In this paper, we design a silicon tuner with TSMC 0.18*um* process. The cost-efficient chip is designed with small area and high gain for a low cost TV receiver within a single silicon area.

II. Proposed Tuner Design

To achieve cost-efficient design, the proposed tuner adopts a single stage conversion for low-IF output. Figure 2 shows the architecture of proposed DTV tuner. The two-step LNA is used to amplify the weak signal from an antenna. The LNA chip is designed with active inductor to reduce the core size.

The mixer is designed with active two-balance structure [1]. If RF input signal and local signal is $V_1=A_1Cos(w_1t)$ and $V_0=A_0Cos(w_0t)$ respectively, after mixing, we can achieve

$$2A_1A_0\cos(\omega_1 t)\cos(\omega_0 t) = A_1A_0[\cos(\omega_1+\omega_0)t+\cos(\omega_1-\omega_0)t] \quad (1)$$

Besides the basic frequency, the additive and differential frequencies generated can be applied to up conversion and down conversion for RF signal.

The mixer can feed two-phased RF signals, and two-phased local frequencies. With two mixers, one can achieve four phased signals. Each mixer can output two basic signals, one differential signal and one additive signals. Then the polyphase filter is used to catch the differential signal to find IF signal.

The local oscillator is designed with a digital-based voltage control oscillator (VCO). The digital VCO consists of the digital to analog conversion and the five-stage ringing oscillator, as shown in Fig. 3. The input digital code with 8 bit can directly control the frequency

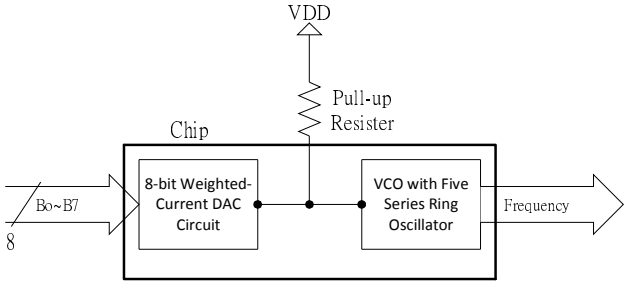

Fig. 3 The digital-based voltage control oscillation.

from 500 to 600 MHz for DTV band in Taiwan. The pull-up resister is used to promote the voltage of DAC output to overcome the threshold of VCO to improve the linearity between voltage and frequency. The VCO is designed with five-stage inverters ringing. A low pass filter is employed at the end of VCO, to smooth the harmonic of ringing oscillator. However, the frequency of VCO may be deviated in process changed. The digital correction with micro-processor can be employed to calibrate the deviation to meet the current DTV band. The

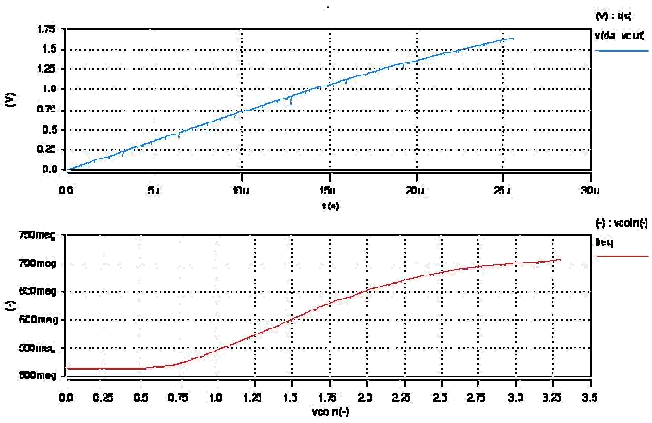

Fig. 4 The simulated results of DAC and VCO.

digital local oscillator can directly select the TV channel with micro processor control.

The digital to analog conversion (DAC) is designed with by the current mode, as shown in Fig 4. P-MOS devices, M16 to M23, are employed to control the current switching. The PMOS driving current is dependent on channel width (W) and length (L), which can be expressed by

$$I_d = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{gs}-V_{thp})^2. \quad (2)$$

The PMOS M16 is LSB, and M23 is MSB. Since PMOS switch turns on when its gate is low, the inverter is used for positive logical control. Also, the inverter can isolate the digital circuit from the analog current to reduce the digital noise. The ration of W/L in each bit is designed to generate 2^n-degree weighting.

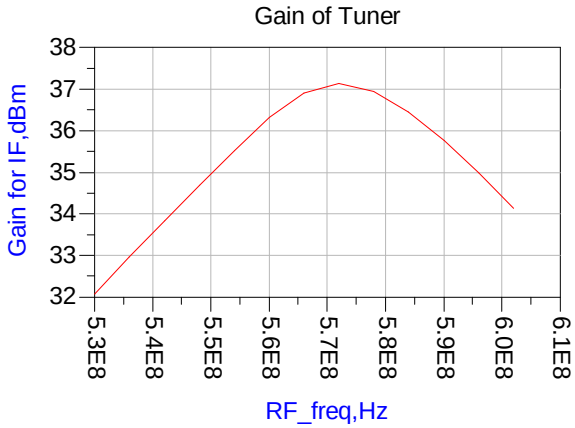

Fig. 5 The frequency response of the proposed tuner.

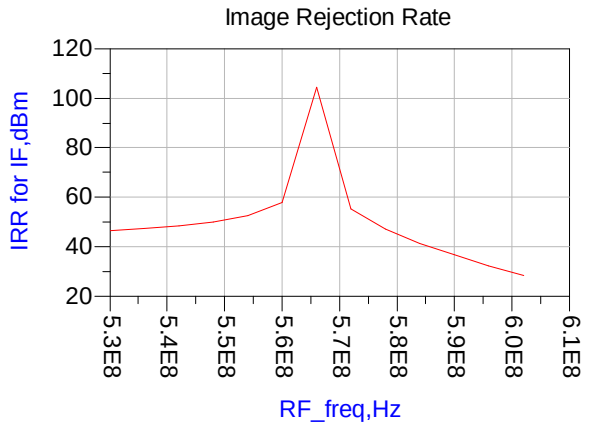

Fig. 6 The image rejection response using proposed tuner

III. Chip Implementation and Comparisons

Based on the proposed circuit in Fig. 2, the tuner chip is realized with TSMC 0.18*um* 1P6M process. First, we individually implement the modules of LNA, mixer, DAC, oscillator and ploy phase filter. Then the entire tuner consists of these modules. With Agilent Advanced Design System (ADS) tool simulations, the results of DAC and VCO are shown in upper and bottom of Fig. 4 respectively. The linearity of DAC is checked by a 8-bit binary counter, where the output voltage is from 0 to 1.6v as the counter from 0 to 255. The VCO output may be not good linearity when the input is at the low and high voltage. In the linearity region, the VCO can generate 530MHz to 680MHz corresponding to the input voltage from 0.75v to 2.5v. To overcome the MOS offset, the pull resistor used in Fig. 3 can increase about 0.75v offset voltage.

The parameters of MOS width/length and resistor are extracted from the results of ADS simulator. The chip layout with the full-custom methodology is according to the MOS parameter. The chip has been verified with LVS and DRC tools in success. Table 1 lists the chip features. The chip can be worked under 1.8V or 3.3V , and the average power dissipation is about 137mW as estimating from Powermill tools. When the operation frequency is from 530 to 602 MHz, the gain can be over 32dBm. Figure 5 shows the gain of the tuner, where the chip can gain about 35dB in average. Figure 6 shows the image rejection power, where the maximum rejection power at the central frequency can achieve about 103dBm, and the image frequency rejection is at least 30dBm among all bands. The image rejection ration (IRR) can achieve about 67dBm in average. The operation band is designed from 530MHz to 602 MHz for the current DTV tuner in Taiwan. The photo for the chip layout is shown in Fig. 10, where the size is 705 * 705 um^2 as included I/O pad.

One can extract the parameters from the post layout to estimate the performance when encountering the process, supply and temperature spread. The tuner is designed by the relative ration of MOS. When the process occurs deviation, but the ration of MOS parameter can be always hold, and the chip feature can be almost kept. With ADS simulations, when the parameter of MOS changes 10%, the gain will degrade 0.8dB at the center frequency. As the power supply has ±10% spread, the chip also can work in normal, but the frequency will shift about 32MHz at maximum. The chip also can work under various temperatures during 0~80°C. However, the center frequency may shift about 1.5MHz, when the temperature changes ±10°C. Table lists the chip features of the proposed tuner.

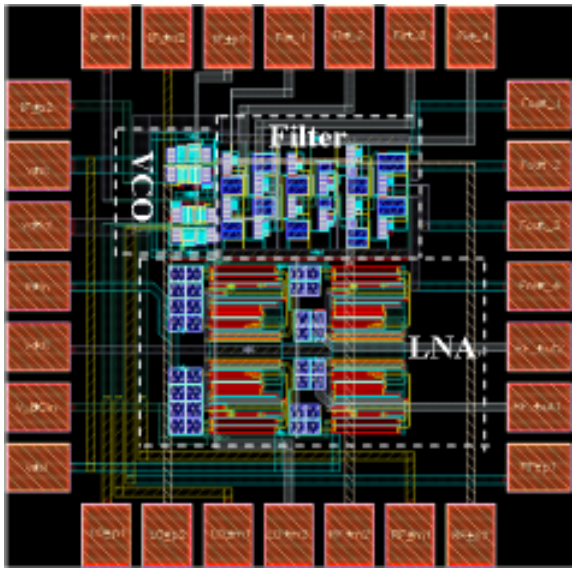

Fig. 7 Photomicrograph of the proposed tuner.

Table 1 Chip Features of the Proposed Tuner

Receiving Frequency	530 to 602 MHz
PDC/Power Supply	136.692 mW/1.8 & 3.3 V
Process	TSMC 18μm 1P6M
Core Area	300 * 365 um^2
Chip Area with PAD	705 * 705 um^2
Gain	32 to 37 dBm
IRR	30 to 103 dBm

Now we evaluate the performance for the proposed tuner with some parameters. (1) The **group delay** is about 0.4~0.6 ns in the DTV band, as shown in Fig. 8. (2) The **stability of filters** operates at entire frequency range, as shown in Fig. 9. These values in operated band all can be over 1, which denote that the tuner can work stably. (3) The **dynamic Range** is measured at IF 36.2 MHz when input power is from -190 dBm to -55 dBm. The dynamic

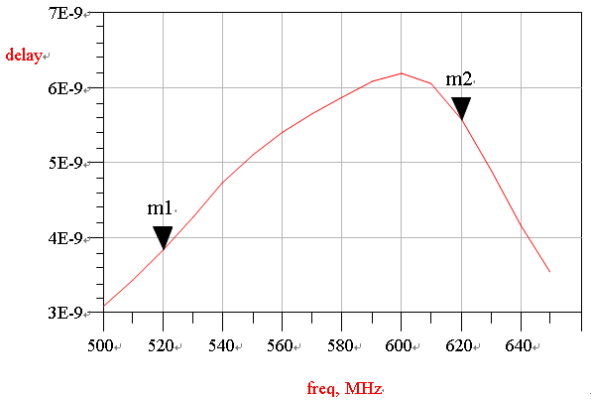

Fig. 8 The group delay of the proposed tuner.

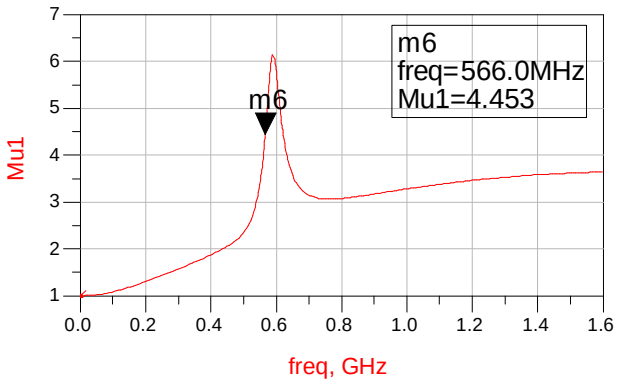

Fig. 9 The stability of filters from IF output ports.

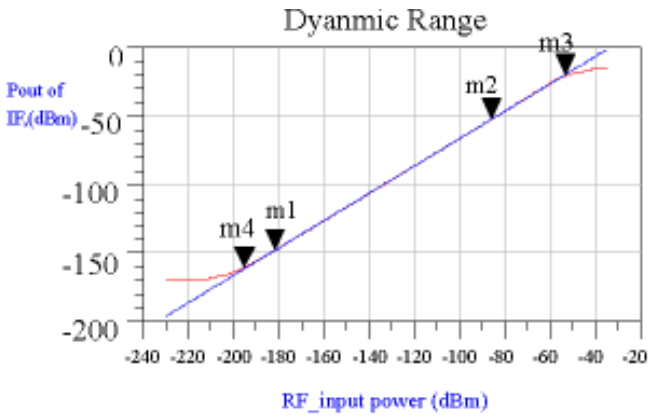

Fig. 10 The dynamic range(RD) of the proposed tuner.

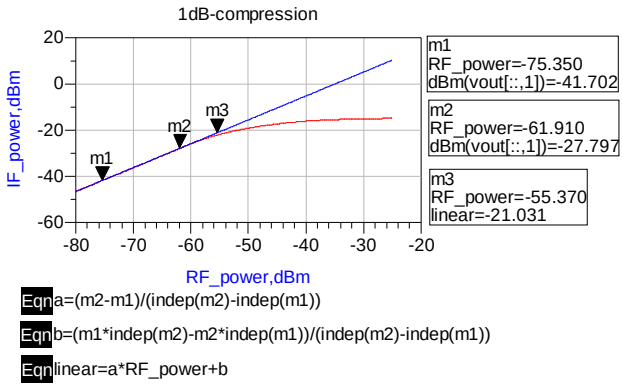

Fig. 11 The linearity evaluation for the proposed filter.

range of proposed tuner is about 135 dBm, as shown in Fig. 10. (4) The **linearity** of filter between input and output is shown in Fig. 11. The points m3 is located at 1dBm gain compression, where the output becomes non-linearity when input power is over –55dBm.

IV. Conclusions

This paper presented a low-cost tuner module for DTV. The chip is successfully implemented with TSMC 0.18*um* process. Comparisons with the existed tuner chips, there are many advantages using this approach. (1) The silicon area can be greatly reduced on-chip. (2) The power dissipation can be much reduced. (3) The chip can be directly controlled by the digital circuit. (4) The chip without using any inductor is easily implemented in silicon chip. When polyphase filter combined with a mixer, the image frequency can be rejected about 67dBm in average for DTV tuner band. With area cost-effective design, the chip size is only 0.49 mm^2 (included I/O pad) and its core size is only 0.11 mm^2 with TSMC 0.18*um*.

With low power and small area, this tuner chip can be embedded to the set-top-box for the DTV system.

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