A Built-in Test Circuit for Injected Charge Tests of Open Defects in CMOS ICs

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Abstract: In this paper, a built-in test circuit for an electrical test method is proposed to detect open defects in CMOS ICs. The test method is based on amount of charge injected from a power supply voltage source. A memory IC is prototyped in which the test circuit is embedded. It is examined experimentally whether an open defect in the IC can be detected with the test circuit. The experimental results show that an open defect in ICs can be detected by the test method.

Keywords-- **CMOS, Open Defect, Electrical Test, Built-in Test Circuit**

1. Introduction

Open defects have often occurred in CMOS logic ICs when they are manufactured by the state-of-art technologies. When they occur in the IC, it is very difficult to detect them owing to low observability and controllability of logic signals in the ICs. It is discussed in this paper how to detect open defects in CMOS ICs.

Open defects are difficult to be detected by measuring output logic values of ICs, since faulty effects caused by them depend on various kinds of factors. They may be detected by supply current test methods. Thus, various kinds of supply current test methods have been proposed. They are classified into IDDQ test methods and IDDT ones that are based on quiescent supply current and transient one of an IC, respectively.

Open defects may not be detected by IDDQ tests, since large quiescent supply current change may not always appear when an open defect is excited. It has been shown that an open defect can generate large IDDT change [1]. It means that IDDT is effective for detecting open defects. Thus, some kinds of IDDT test methods have been proposed [2-4]. Resistive open defects can generate only small delay. They can be detected by IDDT testing, even if deep-submicron CMOS ICs are targeted [4].

Transient supply current can depend on measuring environment. Thus, robust tests based on IDDT testing are very difficult. In order to realize robust tests, IDDT sensors should be implemented inside an IC. Until now, some kinds of IDDT sensors have been proposed [3,4].

The researches on IDDT tests reveal us that electrical testing is effective for open defect detection. Thus, we tried to develop an electrical test method. Change in supply current waveform corresponds to one of the amount of charge supplied from a power supply source. Thus, we have developed a test method based on the amount of the charge [5]. Also, we have examined feasibility of the tests by Spice simulation.

In this paper, we propose a new built-in test circuit of the test method in order to reduce the circuit size. We made a prototype IC in which the test circuit was embedded in order to examine the feasibility of the tests by some experiments. We denote the experimental results in this paper.

2. Test Method Based on Amount of Injected Charge

Whenever an output logic value of a CMOS gate changes, supply current will flow into the gate. Thus, when an input vector is provided to a CMOS circuit, dynamic supply current appears. The dynamic current is caused by penetrating supply current of gates whose output logic values change, and by charging supply one of gates whose output logic level change from a low(*L*) level signal to a high(*H*) level one by the input vector application.

The dynamic current appears within only propagation delay time of the circuit, since the supply current flows during output logic value of a gate changes. The propagation delay time depends on input vectors and the input sequence. The time $t_{PD}(j)$ in Figure 1(b) is the propagation delay time when the j-th test vector ($Tv(j)$) is provided to the circuit of Figure 1(a) after the $(j-1)$-th test vector ($Tv(j-1)$). Thus, dynamic current does not flow after $t_1+t_{PD}(j)$ as shown in Figure 1(b) as I_{DDT}.

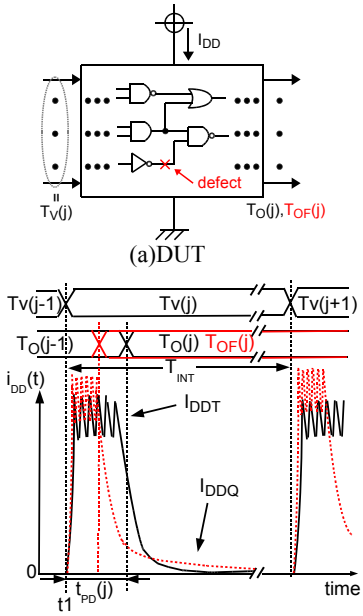


Figure 1. Supply current in CMOS IC.

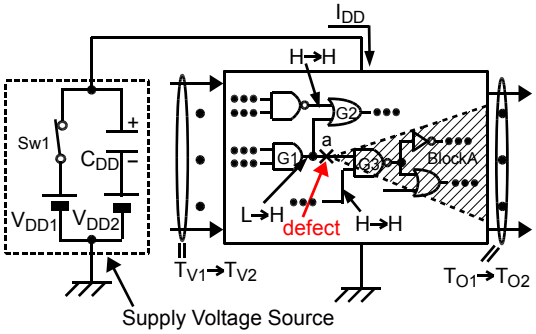


Figure 2. Principle of our test method.

When an open defect occurs, large difference in the IDDT waveform appears. It means that amount of charge supplied from a power supply voltage source to the device under test (DUT) changes. Thus, we developed an electrical test method based on the amount of charge supplied from a power supply source to the DUT [5].

Whenever output logic value of a gate changes, the penetrating supply current will flow in a short time. The output logic value is propagated to a gate. If the output logic value of the gate changes, a penetrating supply current will flow. Also, when the output logic value is charged to an *L* level to an *H* level, supply current will flow so as to charge the output capacitance. The capacitance should be charged so that the voltage across the capacitance can be greater than the threshold voltage of an *H* level signal. When the capacitance can not be charged so as to be in a range of an *H* level signal, the DUT will not work even if the DUT is defect-free. Thus, the capacitance should be charged to a voltage greater than the threshold voltage.

Test principle of our test method is shown in Figure 2. In our test, a source voltage of a DUT is supplied by a supply voltage source circuit. It is made of two kinds of DC voltage source, a capacitor and a switch as shown in Figure 2.

In our tests, source voltage V_{DD} of a DUT is supplied with our power supply voltage source circuit. Also, two test input vectors, *Tv1* and *Tv2*, are used as our test input vectors for the DUT in our tests.

Two kinds of supply voltages, V_{DD1} and V_{DD2}, are provided to our power supply voltage source circuit. V_{DD1} is greater than V_{DD2}.

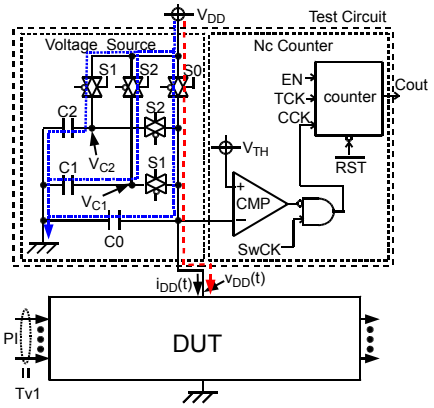
At first, a switch *Sw1* is turned on. The source voltage of the DUT is supplied from V_{DD1}, and a capacitor C_{DD} is charged to be V_{DD1}-V_{DD2}. After that, *Tv1* is provided to the primary input terminals of the DUT. After the output logic values of gates in it are fixed, *Sw1* is turned off and also *Tv2* is provided to the DUT. As a result, I_{DDQ} will flow after I_{DDT} flows. The current is supplied from C_{DD}.

Output logic value of logic gates in the DUT changes and supply current that is not identical to the one of the defect-free DUT flows, when an open defect occurs in the DUT. Thus, the voltage across C_{DD} will be changed by the open defect. In our tests, it is determined by means of the voltage change whether a DUT is defect-free or not.

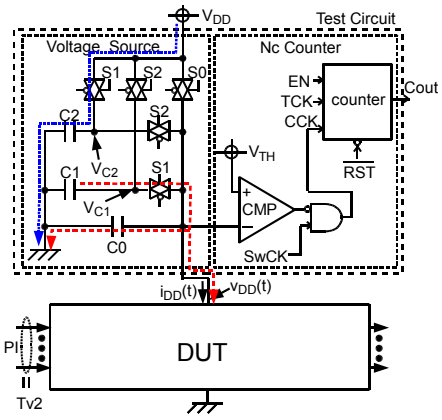
3. Built-in Test Circuit

In order to test a DUT by means of the voltage of C_{DD}, we have developed a test circuit consisting of a power supply voltage source and a counter. The circuit is shown in Figure 3.

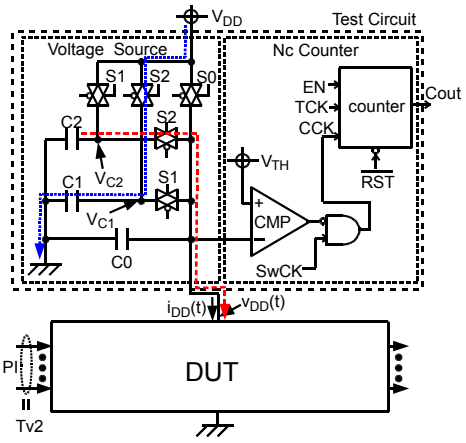
The power supply voltage source, which is depicted as a "Voltage Source", is made of capacitors, analog switches and a switch control circuit. The analog switches are



(a)Phase #1(*S0=S1=S2=H*)



(b)Phase #2(*S0=S2=L,S1=H*)



(c)Phase #3(*S0=S1=L,S2=H*)

Figure 3. Principle of our test method with test circuit.

controlled by control signals of *S0*, *S1* and *S2* that are provided from the switch control circuit.

At first, all of the analog switches are turned on by providing *S0*=*S1*=*S2*=*L* and *Tv1* is provided to a DUT. The dynamic supply current caused by *Tv1* application is supplied from V_{DD}.

After that, *Tv2* is provided to the DUT. By the test input application, I_{DDQ} and I_{DDT} will flow into the DUT. They are supplied from V_{DD}. After output logic values of all of the gates in the DUT are fixed and I_{DDT} disappears, all of the switches are turned off. As a result, a source voltage of the DUT is supplied from only C_0.

However, the source voltage of the DUT will decrease, since the charge in C_0 is not enough large to fix output logic values of the gates in the IC. When the voltage is less than a voltage that is specified as the absolute rating of supply voltage, the DUT do not work, even if it is defect-free. Thus, switches from *S1* to *S2* are turned on serially per a specified time so that the source voltage can not become smaller than the absolute rating voltage.

Source voltage of the DUT will increase by the charge stored in a capacitor turned on. When the voltage at the V_{DD} terminal of the DUT is greater than a threshold voltage V_{th}, it stops to turn on another switch. It is judged whether the voltage is greater than V_{th} with a comparator *CMP*.

The number of the charging until the voltage is greater than V_{th} after the *Tv2* application is counted with a counter in the test circuit. The counter and the charging process are synchronized with a clock signal *TCK*. If Eq.(1) is not satisfied, it is determined to be defective by our test method.

$$N_c = N_{cn} \quad (1)$$

where N_c and N_{cn} are the number of capacitors turned on after providing *Tv2* in the DUT and in the defect-free IC, respectively.

4. Evaluation by Spice Simulation

We designed an SRAM IC of 128 bytes in which a built-in test circuit was embedded with Rohm 0.18μm CMOS process in order to examine whether an open defect in a DUT was detected by our test method.

Our designed test circuit is shown in Figure 4. A circuit made of switches *S3*, *S4*, *S5* and *S6* and capacitors C_{i1}, C_{i2}, C_{i3} and C_{i4} are added to the test circuit shown in Figure 3. But they are turned off in our experiments, since they are not included in the voltage source of Figure 3.

An experimental circuit is shown in Figure 5. The circuit is made of our prototyping IC. Some data are stored in the memory IC with a pattern generator (*PG*). TTL compatible signals of 5V are outputted from *PG*. Thus, 74HC04 SSI ICs are inserted between *PG* and our prototyping IC as level shifters. The following parameters are used in our experiments: V_{th}=1.55V, *BIAS*=0.57V V_{DD0}=3.3V and V_{DD}=1.8V.

The test principle of the circuit is show in Figure 6. Two pattern test input vectors of *Tv1* and *Tv2* are provided to the IC. Before providing *Tv2*, an *H* signal is provided to *S0* before providing *Tv2* in order to charge all of the capacitors in the test circuit. After proving *Tv2*, a positive pulse signal is provided to *S1* and *S2* in order to supplying charge from *C1* and *C2*. An enable signal *EN* and a clock

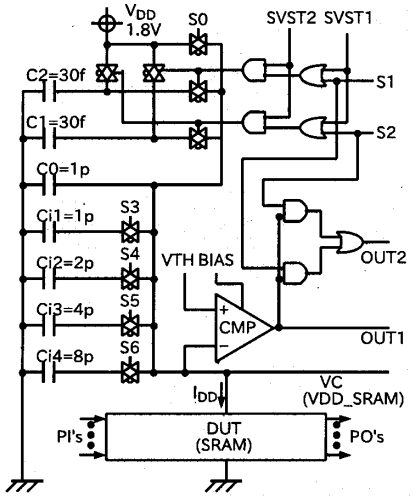


Figure 4. Test circuit embedded in our prototype IC.

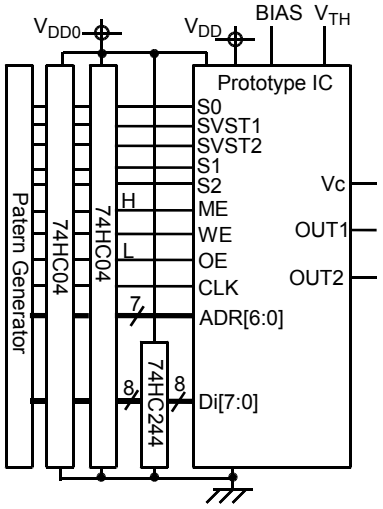


Figure 5. Experimental circuit.

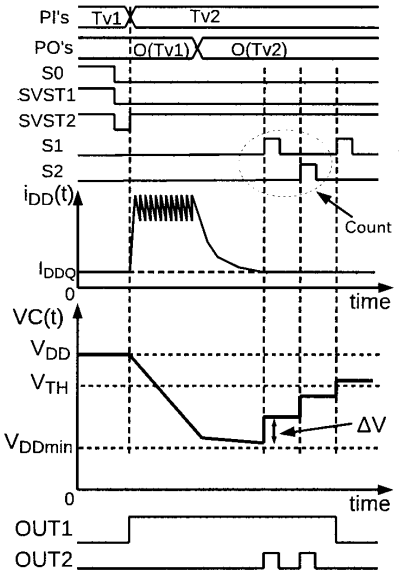
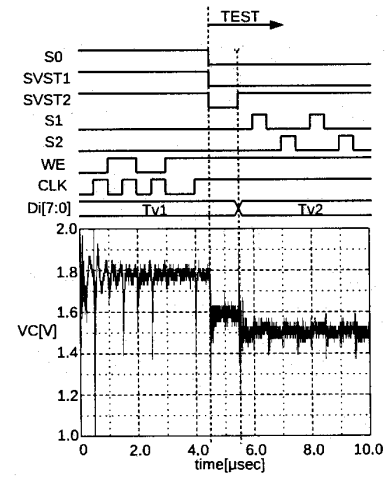
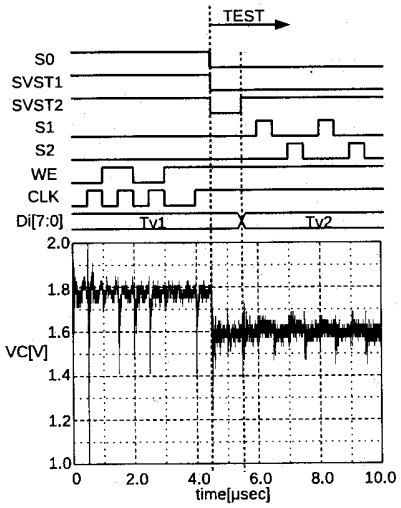


Figure 6. Principle of tests in our prototype IC.



(a)Write *0FH* after *00H*



(b)Write *01H* after *00H*

Figure 7. Waveforms of measured *Vc*.

one *TCK* to the *Nc* counter are outputted from *OUT1* and *OUT2*, respectively.

In our experiments, we write *0xFF* and *0x01* to the memory cells whose address is 0x00, as *Tv1* and *Tv2*, respectively. Larger supply current should flow when *0xFF* is written than when *0x01* is written. Thus, a larger amount of charge should be supplied from a power supply source.

Measured waveforms of *Vc* are shown in Figure 7. In Figure 7(a), *Vc* in the test mode is less than 1.6V. On the other hand, it is greater than 1.6V in Figure 7(b). It reveals us that a larger amount of charge is supplied from our test circuit.

In our experiments, open defects are not inserted into the SRAM IC. However, *Vc* depends on written data. Thus, when open defects occurs in the IC, the amount of charge will change and the defect can be detected by our test method.

In our experiments, *Vc* does not become greater than V_{th}. That is the reason why *C1* and *C2* are smaller than the requested one and amount of charge supplied from the capacitors is not enough large to increase *Vc*. The capacitance depends on a core circuit in an IC. Thus, we should develop a design method of the capacitance.

5. Conclusions

In this paper, we have proposed a built-in test circuit to detect open defects in an IC. Feasibility of the tests is examined for an SRAM IC embedding the test circuit by some experiments. The results show that open defects in a CMOS IC can be detected with the test circuit. It remains to optimize circuit parameters in the test circuit as a future work.

Acknowledgements

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