# 140 GHz CMOS On-chip Dipole Antenna with Optimal Ion-Irradiated-Silicon with Vertical Reflector

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***Abstract*— This paper presents the gain enhancement techniques for a 140 GHz CMOS on-chip antenna. The proposed CMOS on-chip folded dipole antenna is mounted on a metal plate which functions as a reflector. Furthermore, by using ion irradiation which increases the resistivity of the silicon (Si) substrate more than 100 ohms-cm, 5 dB of antenna gain enhancement is achieved. Fabricated in a 40 nm CMOS process, the proposed on-chip antenna achieves an excellent maximum antenna gain of -2.7 dBi at 140 GHz.**

***Keywords— 140 GHz, On-chip antenna, Gain enhancement, CMOS, Ion-irradiation, High resistivity***

## I. INTRODUCTION

Radar technologies that utilize millimeter wave bands offer great possibilities. Due to their broadband nature, millimeter wave bands are suitable for high-precision sensing applications.

In the field of Intelligent Transportation System (ITS), the Advanced Driving Assistant Systems (ADAS) that employ traffic monitoring sensors for detecting pedestrians and bicycles in the intersection area are considered as one of the promising solutions to reduce traffic accidents. The millimeter wave radar sensor is very effective as a traffic monitoring sensor due to its robustness in bad weather and night time conditions. Also, a new 79 GHz radar band (77 - 81 GHz) has recently been allocated for high-resolution radar applications.

Furthermore, various industrial applications such as logistics systems, construction machinery and robots for disaster response are expected to use millimeter wave radars. In these applications, in order to detect humans and small objects within about a 10m maximum range, higher range resolution and fast 3D (three dimensional) scanning radars would be required. For realizing higher range resolution, the use of 140 GHz (136-148.5 GHz) band is attractive option as such wide bandwidth has already been allocated internationally.

In millimeter wave bands above 100 GHz, the connection loss between an off-chip antenna and a CMOS on-chip circuit becomes large. The CMOS on-chip antenna is very effective for solving this issue. Around 60 GHz bands, several on-chip antennas using a CMOS process have been reported [1, 2, 3]. However, they suffer from gain reduction due to low resistivity of the Si substrate. Although an efficiency-enhancement technique of the on-chip antenna using ion irradiation is presented for 60 GHz bands [4], the available gain is not enough for the 140 GHz radar systems.

In this work, we propose a vertical reflecting structure (VRS) using a metal plate that is parallel to the antenna surface under the CMOS on-chip antenna. By providing a unidirectional radiation pattern, the proposed VRS improves the gain of the dipole antenna which is maximized by optimizing the Si substrate thickness. The gain enhancement using ion irradiation is also investigated through both simulation and measurements. Fabricated in a 40 nm CMOS process, the proposed on-chip antenna achieves an excellent maximum antenna gain of -2.7 dBi at 140 GHz as a result of the proposed VRS as well as gain enhancement using ion irradiation.

## II. THE PROPOSED ANTENNA STRUCTURE

In millimeter wave bands, the connection loss between antennas and RF circuits becomes very large as the frequency becomes higher. To realize compact size and high performance modules in 140 GHz bands, on-chip antennas are very attractive because they can minimize the antenna size and the connection loss between antenna and RF circuits.

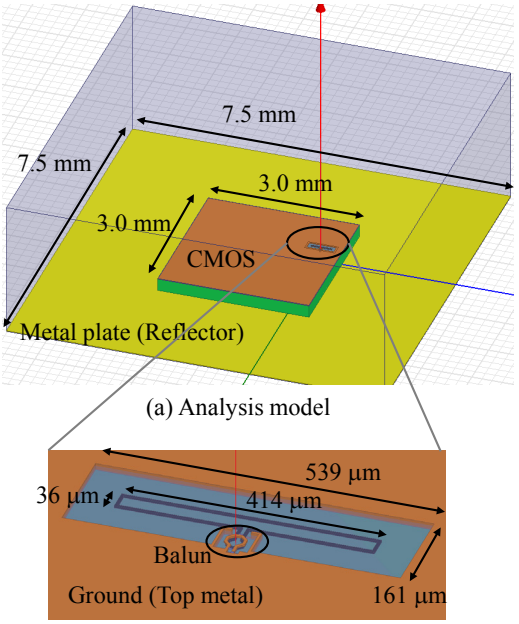
In the deep-submicron CMOS process, it is difficult to obtain a solid ground pattern. Therefore, a differential signal is suitable for an on-chip antenna implemented on a CMOS process. Fig. 1 shows a 140 GHz band CMOS on-chip folded dipole antenna that utilizes the proposed VRS. A 3 mm x 3 mm sized CMOS chip is mounted on a metal plate that operates as a reflector. The size of the antenna core is 414 μm x 36 μm, and the ground aperture size is 539 μm x 161 μm. The antenna element is fabricated on the $SiO_2$ layer, and the width of the dipole antenna is 5 μm. The on-chip antenna offers a unidirectional radiation pattern by the reflector, which increases antenna gain. In order to evaluate the 140 GHz band on-chip antenna by single-ended high frequency probe, an on-chip balun is also integrated. The balun is constructed by an electromagnetic-coupled transformer using the top metal layer (Al) and the underlying metal layer. The midpoint of the differential port is connected to the ground, acting as a virtual ground to maintain good amplitude-phase balance in the differential output signal. The simulated in-band insertion loss of the balun is less than 2 dB, and amplitude and phase errors are less than 0.7 dB and 6 degrees respectively.

In the proposed VRS, to obtain increased antenna gain, the distance from the antenna to the reflector needs to be optimized. Fig. 2 shows the simulated antenna gain over the Si substrate thickness. The silicon substrate is modeled by high permittivity ($\varepsilon_r$ = 11.9) and low resistivity (10 Ω-cm). As

shown in Fig. 2, the Si substrate thickness of 250 µm achieves the maximum antenna gain of -8.7 dBi.

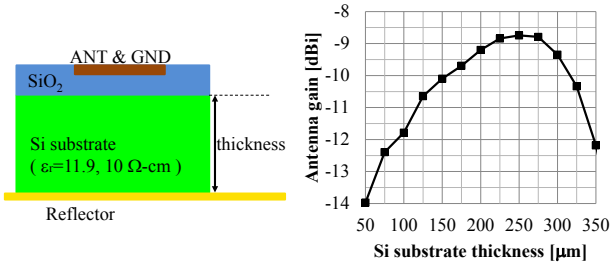
Fig. 3 shows the simulated radiation pattern of the proposed on-chip folded dipole antenna. As expected, it exhibits a unidirectional radiation pattern by virtue of the proposed VRS. The distorted radiation pattern in the Y direction is due to asymmetric antenna positioning on the chip.




(a) Analysis model

(b) Antenna structure

**Fig. 1** Analysis model of an on-chip folded dipole antenna with VRS




(a) Cross section view (b) Simulated results

**Fig. 2** Simulated antenna gain versus Si substrate thickness

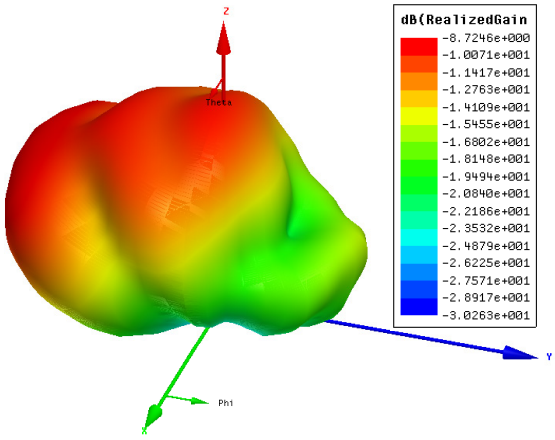


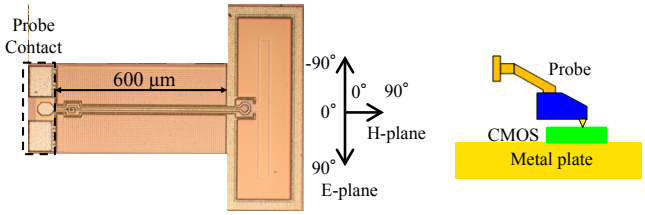

**Fig. 3** Simulated radiation pattern

## III. Measurement Results

Fig. 4 shows the chip photograph and the measurement setting of the fabricated on-chip antenna which used a 40 nm CMOS process. The 140 GHz probe pad is positioned away from the antenna with 600 µm feeding line to minimize influence on the radiation pattern. The Si substrate thickness of the fabricated CMOS chip is 250 µm, which gives maximum antenna gain as explained earlier.

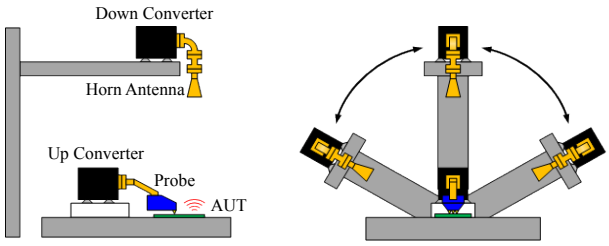
Fig. 5 shows the measurement equipment setup for the on-chip antenna. The radiation pattern of the on-chip antenna is measured by rotating the receiver antenna using a spherical positioner while feeding an RF signal from the high frequency probe to the on-chip antenna.

The input VSWR of the antenna is shown in Fig. 6. It achieves less than 2.1 over the desired band from 136 to 148.5 GHz, which is low enough to measure the power gain of the on-chip antenna. Fig. 7 shows the measured radiation pattern of the fabricated on-chip antenna, which is in agreement with simulation results for both E-plane and H-plane. The ripple of the radiation pattern is due to the influence of the high frequency probe.




(a) Chip photograph (b) Measurement setting

**Fig. 4** Fabricated chip photograph and measurement setting




(a) Side view (b) Front view

**Fig. 5** Measurement equipment setup for the on-chip antenna

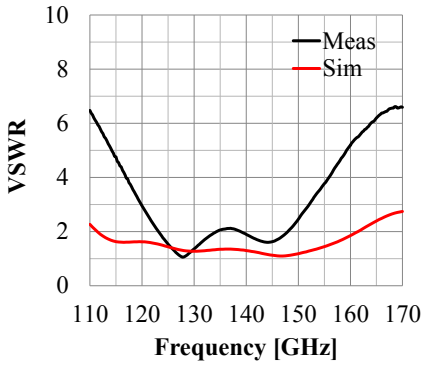
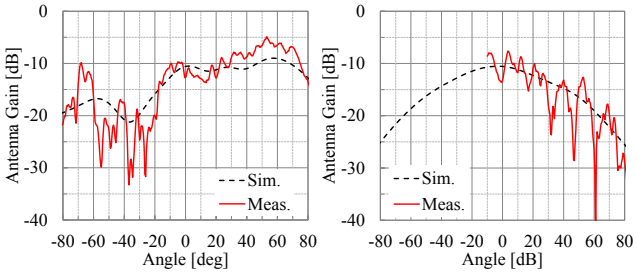



**Fig. 6** Measured input VSWR




(a) E-plane (b) H-plane

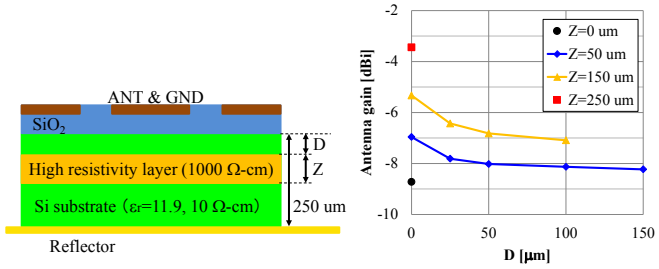
**Fig. 7** Measured radiation pattern of the antenna

## IV. Gain Enhancement by Ion Irradiation

As reported in [4], the ion irradiation of the helium-3 increases the resistivity of the Si substrate which helps in improving the gain of the on-chip antenna. In order to investigate the effect of ion irradiation in the 140 GHz band, simulations with varying resistivity profiles of the Si substrate have been performed. Fig. 8 shows the cross section of the antenna structure and simulation results. The high resistivity region is defined by depth (D) and thickness (Z). The Si substrate thickness and resistivity are set to 250 µm and 10 Ω-cm respectively. The resistivity of the high resistivity layer is set to 1000 Ω-cm, which is realized by the ion irradiation.

Assuming the total thickness of 250 µm, the simulated antenna gain without ion irradiation (D = 0, Z = 0) is -8.7 dBi. With ion irradiation, it improves to -6.8 dBi for D = 50 µm and Z = 150 µm, and -3.4 dBi for D = 0 µm and Z = 250 µm respectively. Even though larger Z is desirable to obtain higher antenna gain, it requires an increased number of ion irradiations, which results in higher cost. According to Fig. 8, it is also known that reducing D is effective to improve the antenna gain.

Measurements have been done for two different conditions and the resistivity profiles in the depth direction are given in Fig. 9. In condition 1, the resistivity of the whole Si substrate is larger than 100 Ω-cm whereas condition 2 has a low resistivity region of less than 100 Ω-cm from D = 60 µm to D = 140 µm. Fig. 10 shows the measured H-plane radiation pattern of the on-chip antenna. As compared to the gain without ion irradiation, condition 2 offers about 2 dB gain improvement. In contrast, condition 1 that has a wider high resistivity region gives about 5 dB gain improvement, achieving an excellent maximum antenna gain of -2.7 dBi at 140 GHz.




(a) Cross section of the antenna (b) Simulated results

**Fig. 8** Simulated antenna gain versus depth and thickness

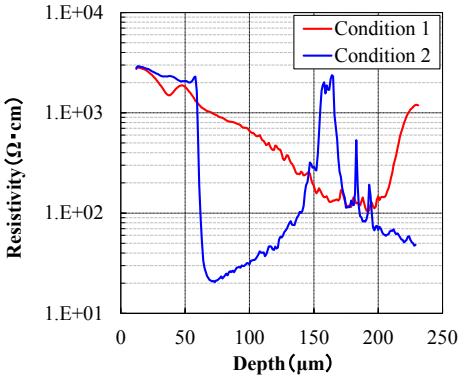



**Fig. 9** Measurement results of ion irradiated resistivity

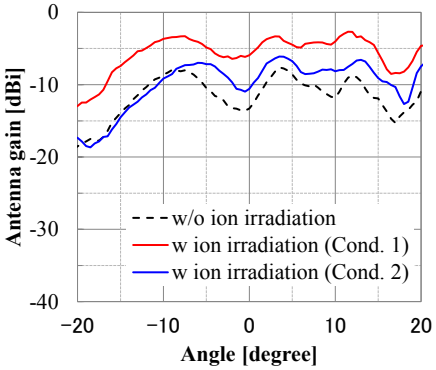



**Fig. 10** Measured radiation pattern with and without ion irradiation

## V. Conclusion

This paper presents gain enhancement techniques for a 140 GHz band CMOS on-chip antenna. The folded dipole antenna with VRS is proposed for achieving improved antenna gain with optimal choice of Si substrate thickness. Furthermore, the gain enhancement using ion irradiation has been demonstrated, showing about 5 dB gain enhancement as a result of increased resistivity in the Si substrate.

## Acknowledgment

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