Open Lead Detection Based on Logical Change Caused by AC Voltage Signal Stimulus

Akira Ono[1], Masahiro Ichimiya[2], Hiroyuki Yotsuyanagi[2], Masao Takagi[1] and Masaki Hashizume[2]
[1] Department of Telecommunications, Takuma National College of Technology
Takuma-cho, Mitoyo, Kagawa 769-1192, Japan
[2] Department of Computer System Engineering, Tokushima University
Minamijousanjima-cho, Tokushima 770-8506, Japan
E-mail: [1]ono@dt.takuma-ct.ac.jp, [2]tume@ee.tokushima-u.ac.jp

Abstract: In this paper, we propose a new test method for detecting an open lead which occurs when an IC is mounted on a printed circuit board. In the method, an open lead is detected by observing output logical change of an open lead detector. Since the test method is a vectorless test one, test generation and test input application are not needed. Testability of the test method is examined by some experiments. The results show that open leads of SSIs and LSIs will be detected by the method.

1. Introduction

Recently, the size of electronic equipments has become smaller. In order to realize the size reduction, fine–pitched LSIs are mounted on a printed circuit boards (PCB). Consequently, opens and shorts have occurred frequently.

Shorts occur by solder bridging between two IC leads. On the other hand, opens occur between a pad on a PCB and an IC lead. The opens are called “open leads” in this paper.

Shorts are detected by conventional test methods [1]. On the other hand, open leads may not be always detected by conventional test methods, because behaviors generated by open leads can not be estimated precisely and controlled. Thus, various kinds of test methods for detecting an open lead have been proposed [2]-[9]. They are classified into two types: the one is based on image processing techniques and the other is electrical testing.

In order to detect open leads, we have proposed two kinds of electrical test methods [8],[9]. The test method proposed in [8] is based on supply current of a logic circuit fabricated on a PCB with CMOS LSIs, which flows when AC electric field is applied from the outside of the circuit.

The test method proposed in [9] is based on supply current of an inverter gate in our test circuit which flows when an AC voltage signal is provided to a targeted lead with a probe. We showed by some experiments that an open lead could be detected by the method.

However, the test methods proposed in [8] and [9] need a current probe for measuring supply current. A current probe is generally expensive. Thus, we propose a new test method for detecting an open lead which does not need a current probe in this paper.

In the new test method, an AC voltage signal whose amplitude is V_{DD} is provided to a targeted lead through a test probe as a test stimulus. It is examined with a logic gate that is used as an open detector whether voltage of the targeted lead is continued to be either H or L level during the test. In the test method, an open lead is detected by means of logical change of the open detector.

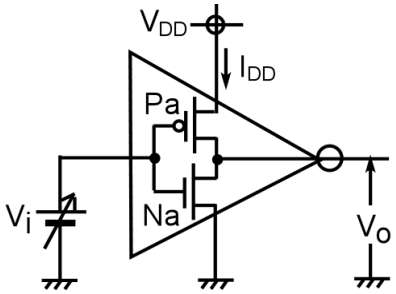
Testability of our test method is examined by some experiments. In this paper, we show the experimental results.

2. Open Lead Detection Method

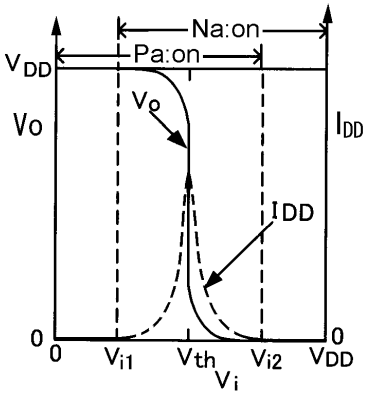
Input/Output voltage characteristics of a CMOS inverter gate is shown in Figure 1. As shown in Figure 1(b), when V_i is either V_{DD} or 0V, supply current of almost zero will flow into the gate. However, if V_i is in the range specified by Eq.(1), large supply current will flow, since both pMOS and nMOS transistors in the gate turn on. The test method proposed in [9] uses this characteristic to detect open leads.

$$V_{i1}<V_i<V_{i2} \quad (1)$$

A test circuit proposed in [9] is shown in Figure 2. In Figure 2, an inverter gate INV is used as an open detector that is called TGATE in this paper. The test circuit consists of an AC voltage source, INV and a resister. v_T of a sine waveform specified by Eq.(2) is supplied from the AC



(a) Measurement Circuit



(b) DC Characteristics

Figure 1. DC Characteristics of CMOS Inverter Gate

voltage source to a targeted lead with a test probe as shown in Figure 2.

$$v_T=V_{DD}\sin(2\cdot\pi\cdot f_T\cdot t) \quad (2)$$

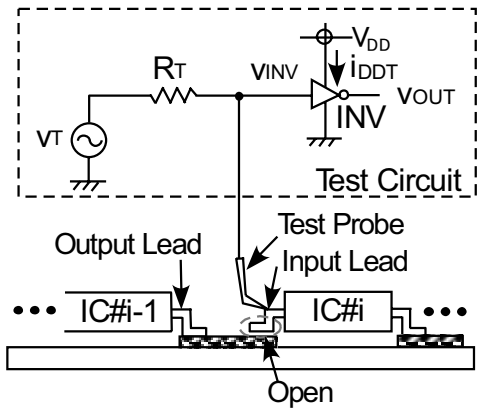


Figure 2. Test Circuit for Our Test Method

When an open lead does not occur at the targeted lead, supply current of TGATE will not flow, since V_i is either H or L. On the other hand, when an open lead occurs, V_i is within the range specified by Eq.(1) and large supply current flows. By means of the supply current change, the open lead is attempted to be detected in [9].

In our new test method, we use the same test circuit as the one shown in Figure 2 and measure v_{OUT} instead of i_{DDT} in order to detect the open lead.

When no open lead occurs at a targeted lead, input voltage of INV is either H or L level regardless of v_T. Thus, v_{OUT} will be either H or L level even if v_T is provided.

On the other hand, when an open lead occurs at the targeted lead, v_{INV} will change in time according to v_T. Thus, v_{OUT} will not be continued to be a constant value. By means of this logical change, the open lead is attempted to be detected. That is, if logic value of v_{OUT} changes in time, it is determined by our test method that an open lead occurs at the targeted lead.

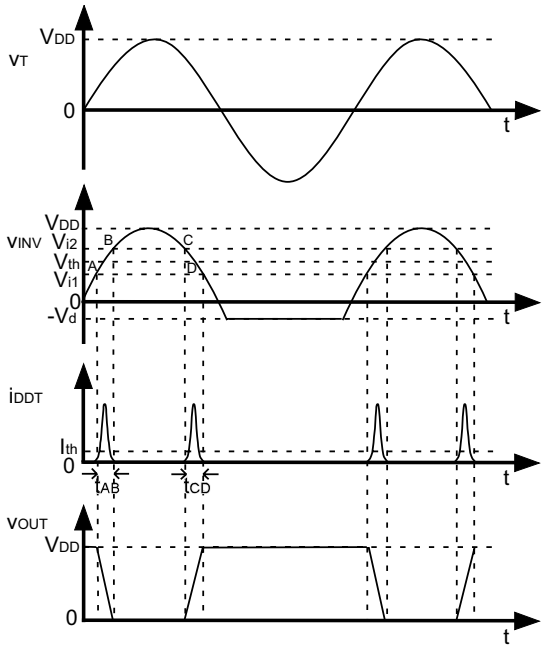


Figure 3. v_{OUT} in Our Tests of Faulty Circuit.

Examples of the waveforms of v_T, v_{INV}, i_{DDT} and v_{OUT} which appear when an open lead occurs are shown in Figure 3. As shown in Figure 3, when V_i is in the range specified by Eq.(1), elevated i_{DDT} flows. Furthermore, logical changes appear when the open lead occurs.

On the other hand, when an open lead does not occur at the targeted lead, no logical change will appear at the output of TGATE, since v_{INV} is either H or L level that is provided from the targeted lead during the test.

The test method is a vectorless test one, since logical changes will appear regardless of logic values from the output lead when an open lead occurs. Thus, test generation and test input application are not needed. Also, an expensive measurement tool such as a current probe is not needed. Thus, it is expected that a tester of low price will be developed.

3. Evaluation by Experiments

In order to examine feasibility of our new test method by some experiments, open leads of an SSI and LSIs are targeted. Our experimental circuit is shown in Figures 4 and 5.

In the test circuit, TC74HC04AP and TC74HC00AP are used as TGATE and IC#i-1 in Figure 2, respectively. An SSI of TC74HC00AF and CPLD LSI's of EPM7128SQC100-15 and EPM7064AETC100-10 are used as targeted IC, IC#i, having an open lead. As shown in Figure 5, an adder circuit is programmed in the CPLD LSIs.

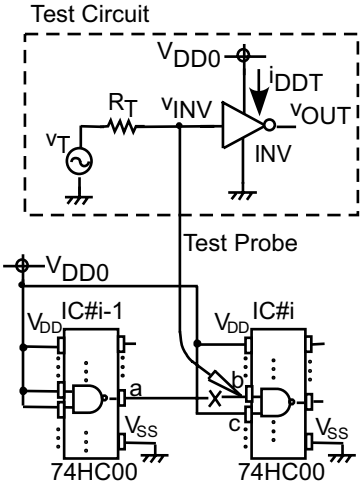


Figure 4. Experimental Circuit for SSI

In our experiments, f_T is 1 kHz and R_T is 1kΩ. i_{DDT} is measured with a current probe. A test probe is attached to the top of a targeted lead directly with a probe holder shown in Figure 6. The contact pressure is about 56gw.

Measured waveforms are shown in Figures 7, 8 and 9. As shown in Figures 7(b), 8(b) and 9(b), when no open lead occurs at the targeted lead, no logical change will appear in v_{OUT}. On the other hand, as shown in Figures 7(a), 8(a) and 9(a), when an open lead occurs at the targeted lead, logical

change appears in v_{OUT} during the test. Thus, the open leads are detected by using our new test method.

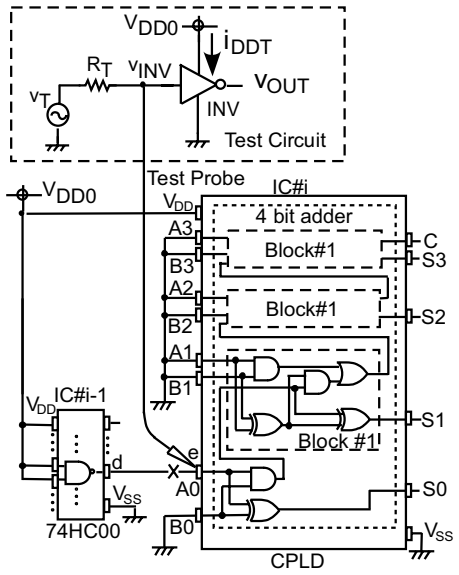
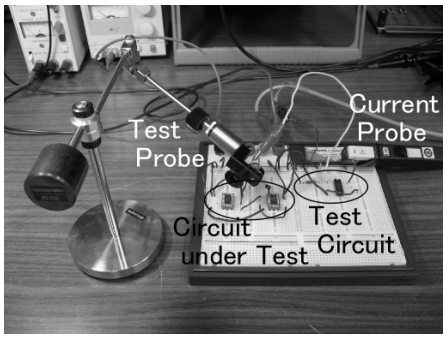
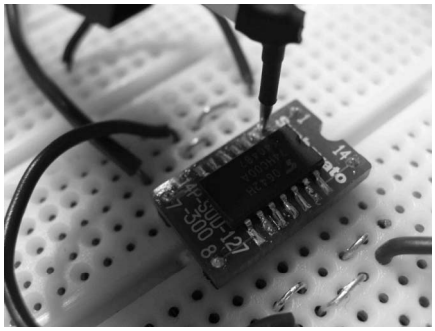


Figure 5. Open Lead Detection of CPLD LSIs.



(a) Equipment for Test Probe Attachment



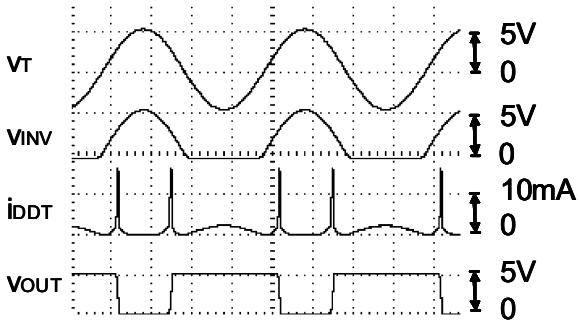
(b) Test Probe Attachment

Figure 6. Attachment of Test Probe

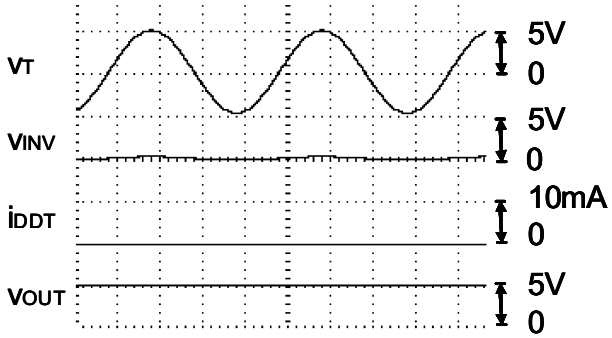
4. Conclusion

In this paper, we have proposed a new test method for detecting an open lead. In the test method, an open lead is detected by monitoring output logical change of a logic gate that is used as an open lead detector. We have shown by some experiments that an open lead of SSIs and CPLD LSIs are detected by the test method.

Test speed of this test method has not been evaluated. It remains as one of future works to evaluate test speed.



(a)Faulty Circuit



(b)Defect-free Circuit

Figure 7. Open Lead Detection of SSI

References

[1] H. Bleeker, P. van den Eijnden, and F. de Jong, Boundary-Scan Test: A Practical Approach, Kluwer Academic Publishers, 1993.

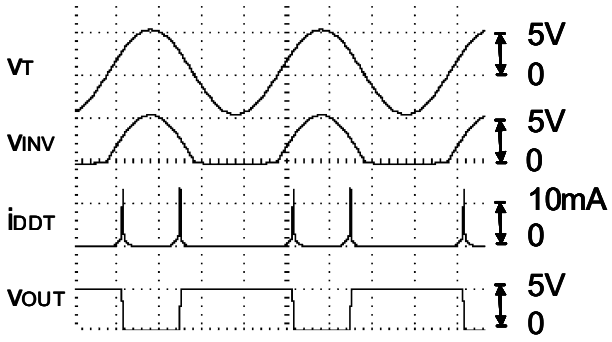
[2] C. Vaucher, "Electrical Test: Where are we and where are we going?" Proc. of ECWC8, pp.H3-3-1-3-3-6, Sept. 1999.

[3] Ted. T. Turner, "Capacitive Leadframe Testing", Proc. of ITC-96, p.925, Oct. 1996.

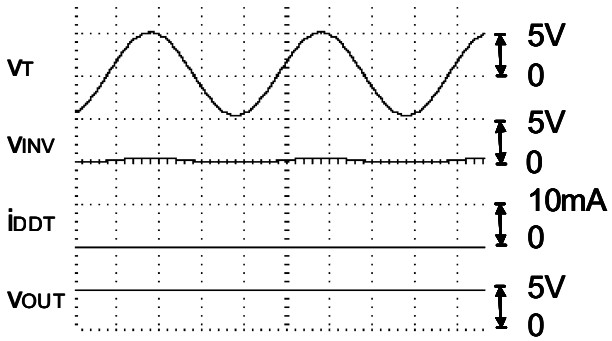
[4] Jack Ferguson, "High Fault Coverage of In-Circuit IC Pin Faults with a Vectorless Test Technique using Parasitic Transistors", Proc. of ITC-96, p.926, Oct. 1996.

[5] Joe Wrinn, "Two New Techniques for Identifying Opens on Printed Circuit Boards: Analog Junction Test and Radio Frequency Induction Test", Proc. of ITC-96, p.927, Oct. 1996.

[6] Anthony J. Suto, “Analog AC Harmonic Method for Detecting Solder Opens”, Proc. of ITC-96, p.928, Oct. 1996.
[7] Stig Oresjo, “Unpowered Opens Test with X-Ray Laminography”, Proc. of ITC-96, p.929, Oct. 1996.
[8] Masao Takagi, Masaki Hashizume, Masahiro Ichimiya, Hiroyuki Yotsuyanagi and Takeomi Tamesada, “Lead Open Detection Based on Supply Current of CMOS LSIs,” IEICE Trans. fundamentals, vol. E87-A, no. 6, pp.1330-1337, June 2004.
[9] Akira Ono, Masaki Hashizume, Masahiro Ichimiya and Hiroyuki Yotsuyanagi, “Open Lead Detection of CMOS ICs by Low Pressure Probing”, Proc. of ICEP2007, pp.359-364, 2007.

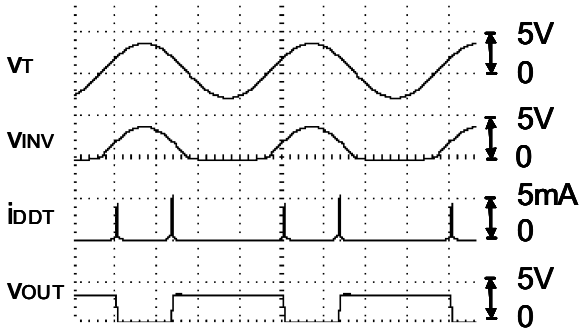


(a) Faulty Circuit

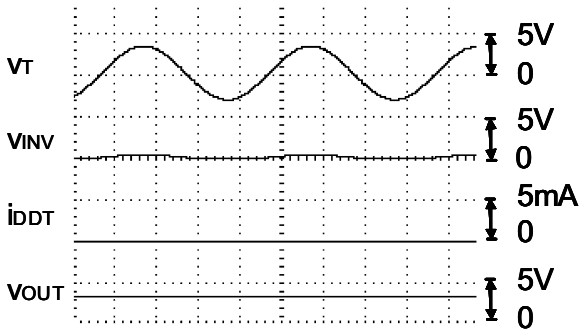


(b) Defect-free Circuit

Figure 8. Open Lead Detection in 5V CPLD



(a) Faulty Circuit



(b) Defect-free Circuit

Figure 9. Open Lead Detection in 3.3V CPLD