A Reconfigurable CMOS Low Noise Amplifier for Wireless LAN Applications

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Abstract: This paper presents the designed and implemented CMOS Low Noise Amplifier (LNA) for multiband operation in TSMC 0.18 μm process. To operate in multibands and multistandards, switched inductor and switched capacitor array are used in input and output signal paths. Due to filtering characteristic of input stage, the LNA can suppress spurious signal effectively. The designed reconfigurable LNA is targeted to IEEE 802.11n application which operates in dual band: 2.4~2.485 GHz and 5.15~ 5.825 GHz. At each frequency mode; 2.4 GHz, 5.25 GHz and 5.75 GHz, gains are more than 12 dB while NFs are kept less than 2.2 dB. The LNA can be optimized the performance to each operation frequency by using LC resonant circuits and capacitor array networks.

1. Introduction

In the considerations for the design of wireless communication systems, the importance of reconfigurability or multiband operation grows than ever. In the first stage, the design method of RF system having different signal paths on operation frequencies is used for a solution of multiband RF system. However, large chip size remains on demerit. For the high integrated RF system design, a single path and multiband RFICs design becomes the primary design goal.

In the purpose of multiband selection and high integration, several matching methods have been published: concurrent matching [1], switched LC matching [2], and wideband matching [3]. Although concurrent matched system can deal with various signals in single path without any controller, it accepts spurious signal at the same time. So linearity of RF system is degraded. Switched LC matching accepts desire signal selectively by changing the operation mode, however insertion loss of switch transistor is subsisted and system noise performance get worse. Wideband matching having non-exclusive characteristic within its operation frequency receives unwanted interferers with the desired signal simultaneously.

In this paper, a reconfigurable matching method is proposed. By removing the switch component in signal paths, noise performance can be improved and by turning on and off input bias voltages frequency selectivity is achieved. The multiband LNA using the proposed matching method is designed in 0.18 um CMOS technology. The proposed LNA applies the merit of concurrent matching and selectivity of receiving signal to the multiband operation. Figure 1 shows the single path multiband RF receiver and the proposed CMOS LNA.

This paper is organized as follows: Section II covers the operation principle of the reconfigurable LNA. Section III explains the design process of the proposed LNA and shows the performance results. Finally, Section IV is the conclusion of this paper.

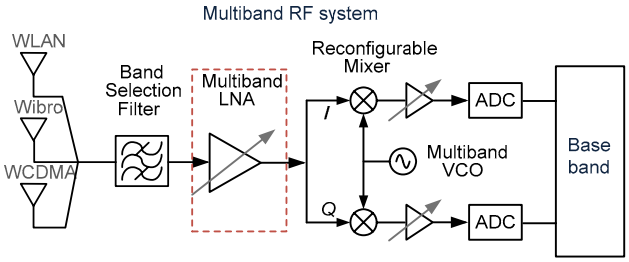


Figure 1. The block diagram of the single path multiband RF receiver

2. Operation Principle of the Reconfigurable LNA

For the selection of operation frequency, switched gate bias and switched inductor and capacitor networks are used. The resonance frequency of LNA is determined by LC network. The schematic of the proposed input matching network is shown in Figure 2.

Degeneration inductor provides input and noise matching simultaneously [4-5], the proposed LNA has optimum input and noise matching characteristic. In the input matching network, SW_1, SW_2, and SW_3 make reconfigurability of the LNA. As SW_1 and SW_2 are turned on and off alternatively, the LNA selects the operation frequency mode; low frequency or high frequency mode. When the SW_1 is turned on and SW_2 is turned off, the LNA operates in low frequency mode and input matching network is composed with series connection of L_1 and L_2.

The switched inductor and switched capacitor array can maximize the reconfigurability of circuit due to the dependence of resonance frequency on LC networks. By adding capacitor array, from C_1 to C_5 in the input and output matching network, operation frequency can be feasible to fine-tuning from 5.2 to 5.75 GHz.

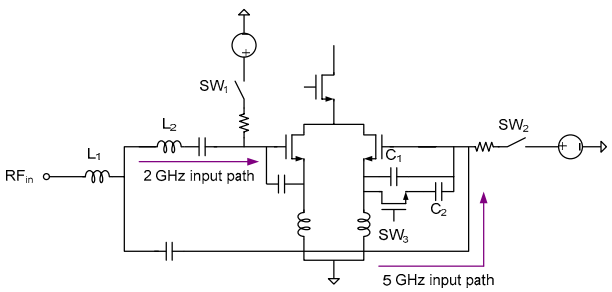
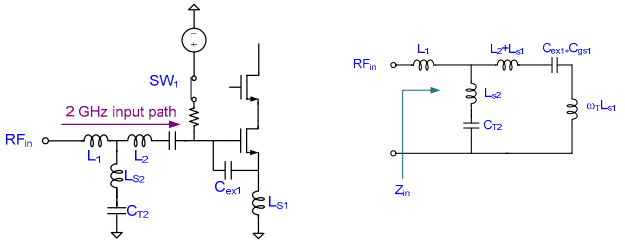


Figure 2. The reconfigurable input matching network



(a) Input matching network (b) equivalent circuit

Figure 3. Input matching network at low frequency mode

The low frequency mode input matching network is presented in Figure 3.

Input impedance at low frequency mode is expressed as equation (1);

$$Z_{in} = sL_1 + \left(\left(s(L_2 + L_{s1}) + \frac{1}{sC_{T1}} + \frac{g_m \cdot L_{s1}}{C_{T1}} \right) + \left\| \left(sL_{s2} + \frac{1}{sC_{T2}} \right) \right. \right) \quad (1)$$

where $C_{T1} = C_{gs1} + C_{ex1}$ and $C_{T2} = C_{gs2} + C_{array\_in}$. With long derivation and approximation, real part of input impedance and resonant frequency can be obtained.

$$\mathrm{Re}[Z_{in}] \approx \frac{g_m \cdot L_{s1}}{C_{T1}} = \frac{g_m \cdot L_{s1}}{C_{gs1} + C_{ex1}} \quad (2)$$

By selecting degeneration inductor value, L_{s1}, equal to source impedance and optimum source impedance, the proposed LNA fulfills optimum noise and input matching conditions.

Figure 4 shows the input matching networks of the designed LNA at high frequency mode.

Input impedance at high frequency mode is expressed as equation (3);

$$Z_{in} = sL_1 + \left(\left(sL_{s2} + \frac{1}{sC_{T2}} + \frac{g_m \cdot L_{s2}}{C_{T2}} \right) + \left\| \left(sL_T + \frac{1}{sC_{T1}} \right) \right. \right) \quad (3)$$

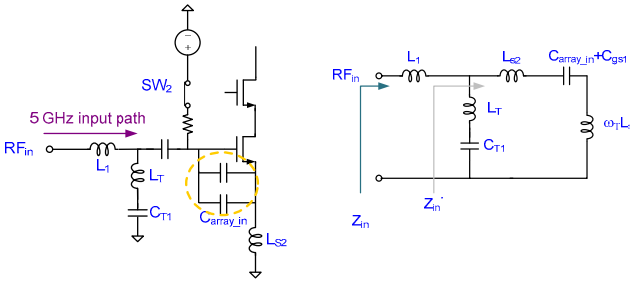
Real part of input impedance and resonant frequency can be obtained.

$$\mathrm{Re}[Z_{in}] \approx \frac{g_m \cdot L_{s2}}{C_{T2}} = \frac{g_m \cdot L_{s2}}{C_{gs2} + C_{array\_in}} \quad (4)$$

By selecting degeneration inductor value, L_{s2}, equal to source impedance and optimum source impedance and by turning on and off SW_3, the proposed LNA fulfills optimum noise and input matching conditions in 5.15~5.85 GHz band.

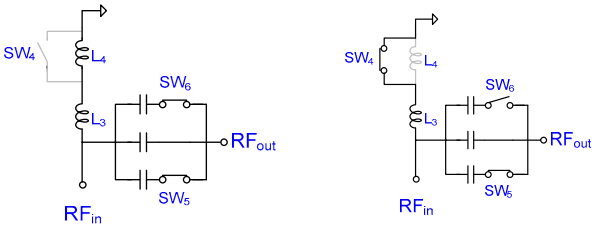
The seriese LC resonance circuit in signal path is useful to reduce negative influence of the spurious signal. With filtering characteristic, high frequency spurious and low frequency spurious are bypassed through seriese $L_{S2}C_{T2}$ resonance circuit and L_TC_{T1} resonance circuit respectively at low mode and high mode operation.

The output matching networks, shown in Figure 5, use switched inductor and capacitor array network.



(a) Input matching network (b) equivalent circuit

Figure 4. Input matching network at high frequency mode



(a) Low frequency mode (b) High frequency mode

Figure 5. Output matching network of the LNA

By turning on and off SW_4, SW_5, and SW_6, the LNA selects operation frequency. While SW_4 is turned off, output load forms series connection of L_3 and L_4 and operates in 2.4 GHz. When SW_4 is turned on, output load is formed series connection of R_{sw} and L_3 and operates in 5.15~5.75 GHz. Similar to input matching network, operation frequencies in high frequency mode can be fine-tuned by capacitor array network.

3. LNA Design and Performance Results

The reconfigurable LNA is designed in 0.18 um CMOS technology.The completed schematic of the designed LNA is shown in Figure 6, and it composed with cascode amplifier, input/output matching networks for multiband operation, fine-tunning capacitor arrays, and degeneration inductors. The designed reconfigurable LNA is targeted to IEEE 802.11n application which operates in dual band: 2.4~2.485 GHz and 5.15~ 5.825 GHz.

Cascode structure is an effective method for reverse isolation, so good input and output matching can be achieved separately. With on and off operation of SW_1 and SW_2, signal paths of low and high frequency mode are selected and the operation frequency is 2.4 GHz 5.25 GHz, and 5.75 GHz. When SW_1 is turned on and SW_2 is turned off, series connection of L_1, L_2, C_{ex1}, and L_{s1} forms input matching network and operation frequency is 2.4 GHz band. On the contrary, while SW_1 is turned off and SW_2 is turned on, series connection of L_1, C_{array_in}, and L_{s2} forms input matching network and operation frequency is 5.15~5.85 GHz band. In 5.15~5.85 GHz band, there are several subcarriers, hence, fine-tuning method are required to control operation frequency delicately. In the proposed LNA, capacitor array networks are used for frequency fine-tuning. At high frequency mode in input stage, if SW_3 is turned on, operation frequency is fixed to 5.25 GHz, and

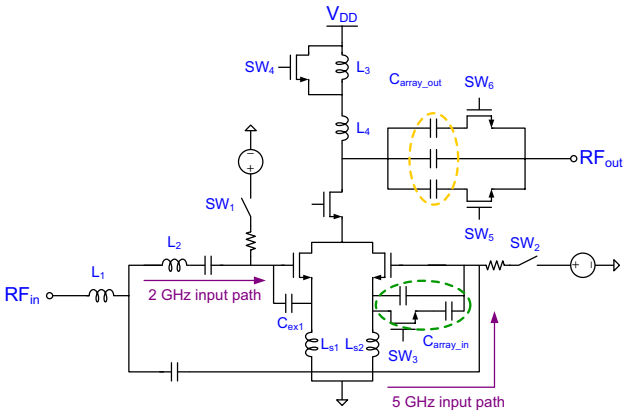


Figure 6. The schematic of the reconfigurable LNA

while SW_3 is turned off operation frequency is fixed to 5.75 GHz. At high frequency mode in input stage, if SW_3 is turned on, operation frequency is fixed to 5.25 GHz, and while SW_3 is turned off operation frequency is fixed to 5.75 GHz. By using capacitor array network, fine-tuned operation is realized in high frequency mode.

The reconfigurable LNA for wireless LAN applications was simulated by spectre RF simulator with 0.18 um CMOS library. The simulated LNA was targeted IEEE 802.11n standard of which operation frequency is 2.4 GHz and 5.15~5.85 GHz band. The current consumptions of the proposed LNA at low and high frequency mode are 2.86mA and 5.1mA with 1.5 V supply voltage, respectively.

As shown in Figure 7 and Figure 8, input and output return losses within its operation frequency are less than -15 dB. At each frequency mode; 2.4 GHz, 5.25 GHz and 5.75 GHz, gains are more than 12 dB while NFs are kept less than 2.2 dB. The IIP3s are -7.17 dBm and -7.09 dBm within its operation frequencies. The LNA can be optimized the performance to each operation frequency by using LC resonant circuits and capacitor array networks.

The chip die photo of the implemented LNA is shown in Figure 11, and the dimension of the reconfigurable LNA is 960 X860 um^2. The performance results are summarized in Table. 1.

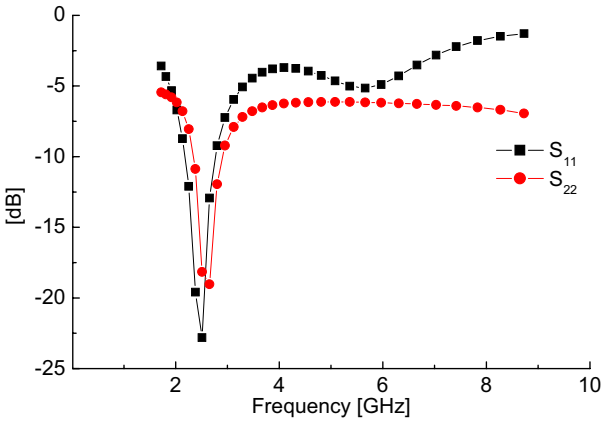


Figure 7. Input and output return loss at low frequency mode

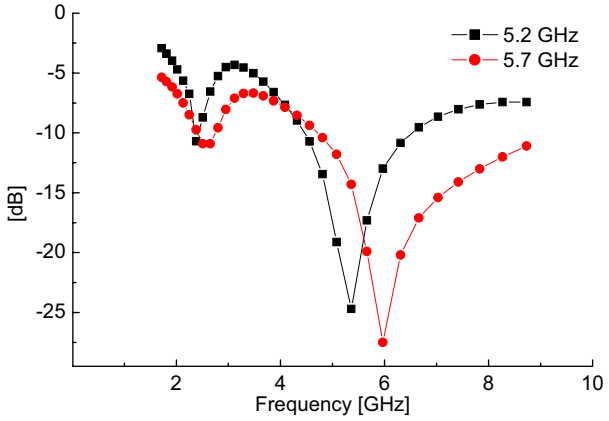


Figure 8. Input return losses of 5.25 GHz and 5.75 GHz operation

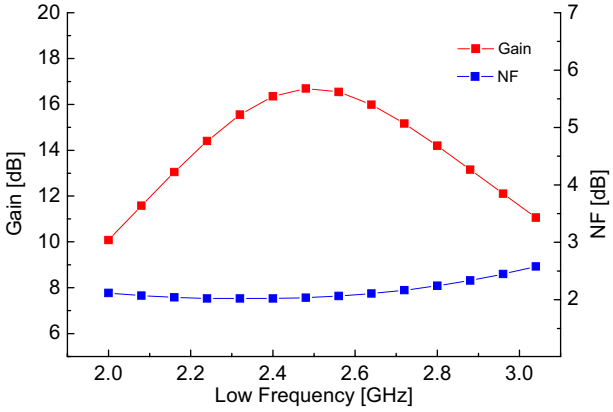


Figure 9. Gain and NF at low frequency mode

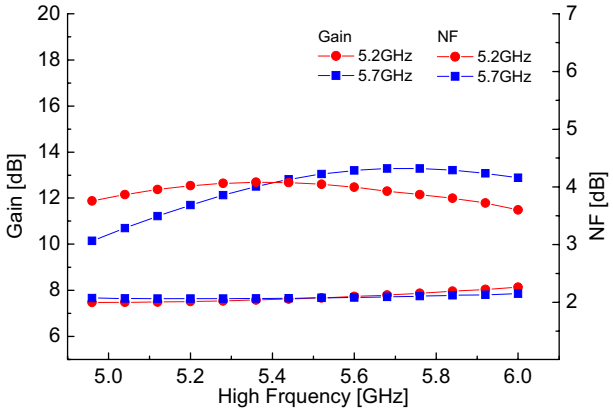


Figure 10. Gain and NF at high frequency mode

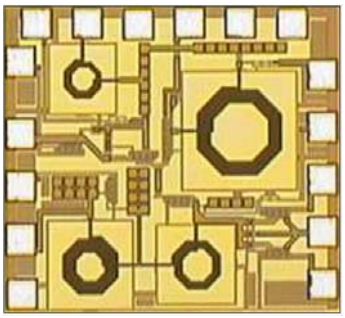


Figure 11. The chip die photo of the implemented LNA

4. Conclusion

In this paper, we proposed reconfigurable LNA with multiband operation characteristic. The proposed LNA is designed and implemented in 0.18 um CMOS process for IEEE 802.11n standard. The designed LNA is consisted of fully on-chip components. To accomplish the multiband operation, series LC resonant circuits, switched inductor, and capacitor array networks are used in input and output matching network. Owing to filtering characteristic of input stage, the LNA can suppress spurious signal effectively.

Operation mode	Low Freq.	High Frqe.	
Freq. [GHz]	2.4	5.25	5.75
Power consumption [mW]	4.3	7.65	7.65
Supply voltage [V]	1.2	1.2	1.2
S11 [dB]	<-15	<-15	<-15
Gain [dB]	16.5	12.89	13.4
NF [dB]	2.17	2.09	2.28
Input IIP3 [dBm]	-7.17	-7.09	-8.13
Technology	0.18 um CMOS		

Table 1. Performance summary

Acknowledgement

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