An Efficient Design Methodology of Serial Concatenate Coding Scheme for CATV Transmission System

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Abstract: This paper describes the design methodology of serial concatenate of extended RS code, trellis coded modulation with 64-/256-QAM, based upon testing and characterization of cable systems.
In implementing the cable modem, there are some problems to fabricate and fitting on FPGA chip. First, many clocks are needed in implementing cable modem because of different code rate and different modulation types. To reduce the number of clocks, we use the two memories, which are different clock speed for reading and writing data. Second, this system lost the bit-synchronization and frame-synchronization in decoder, the system recognizes that all data is error. This paper solves the problems by using simple 5-stage registers and unique sync-word.
Based on solutions for about problems, the cable modem is fabricated on FPGA chip name as Vertex II pro xc2vp30-5 by Xilinx, and we confirmed the effectiveness of the results.

1. Introduction

The ITU-T Recommendation J-38 Annex B describes the frame structure, channel coding, and channel modulation for a digital multi-service television distribution system by cable networks. This paper is focusing only on the forward error correction(FEC) and digital modem part and its implementation. The cable transmission system mainly is composed by serial concatenate of extended Reed-Solomon (e-RS) and convolutional code (CC). This paper analyzed the BER performance of cable transmission system by fixed-point simulation and implemented Field Programmable Gate Array (FPGA) chip.

In implementing the cable modem, there are some problems to fabricate and fitting on FPGA chip. First, many clocks are needed in implementing cable modem because of different code rate and different modulation types. To reduce the number of clocks, we use the two memories, which are different clock speed for reading and writing data. Second, appling punctured convolutional codes to TCM by puncturing a standard rate 1/2 binary convolutional code (BCC) is to achieve fractional rate k/n throughput, where rate k/n can be any desired value less than one. If demodulated symbols does not synchronized to punctured coded pattern that is branch coded word in trellis diagram, we could not find frame synchronization pattern which provide synchronized e-RS decoding, de-interleaving, de-randomizing. This paper propose the sync-word detection algorithm using a simple 5-stage register and FEC frame sync trailer to solve the punctured coded pattern synchronization and frame synchronization together.

This work was supported by Defense Acquisition Program Administration and Agency for Development under the contract UD070054AD

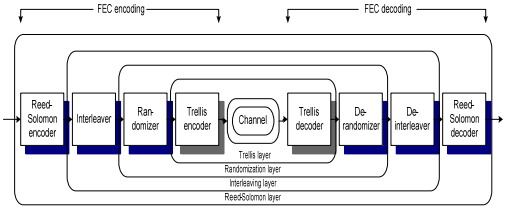


Figure 1. Model of FEC for CATV down stream channel.

Based on solutions for above problems, the cable modem is fabricated on FPGA chip name as Vertex II pro xc2vp30-5 by Xilinx, and we confirmed the effectiveness of the results.

2. FEC for CATV Down Stream

The Forward Error Correction(FEC) definition is composed of four processing layers, as illustrated in Figure 1.
The FEC section uses various types of error correcting algorithms and interleaving techniques to transport data reliably over the cable channel. Table 1 is shown the list of system spec.

Table 1. The list of system spec.

Parameter	Algorithm	Specification
Outer code	Extended RS	(128,122,3)
Inner code	64-QAM mode	TCM with punctured coding rate of 4/5
	256-QAM mode	TCM with punctured coding rate of 19/20
Interleaving	Convolutional interleaving	I=128, J=1
Randomizer	3-stage randomizer	$f(x) = x^3 + x + \alpha^2$
TCM decoder	Number of quantized bits of I/Q channel received symbol	8 bits
	Number of quantized bits of branch/path metric	9 bits
	Trace back method	3-point trace back method

3. Result of Simulation

The Figure. 2 shows the results of simulation of TCM. In this Section, we analyzed the BER performance for TCM with 64-QAM mode and 256-QAM mode.

As shown in Figure. 2, BER performance of the trellis coded 64-QAM is better than that of trellis coded 64-QAM about EbNo of 5 [dB] in Gaussian noise channel.

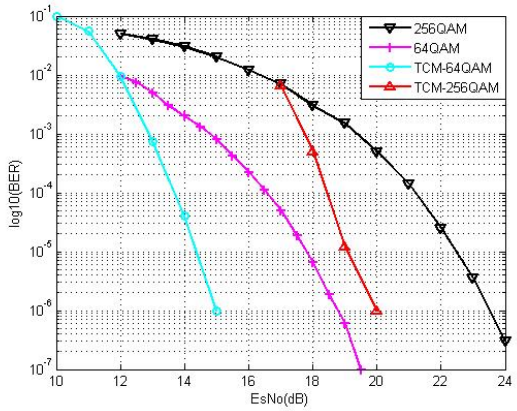
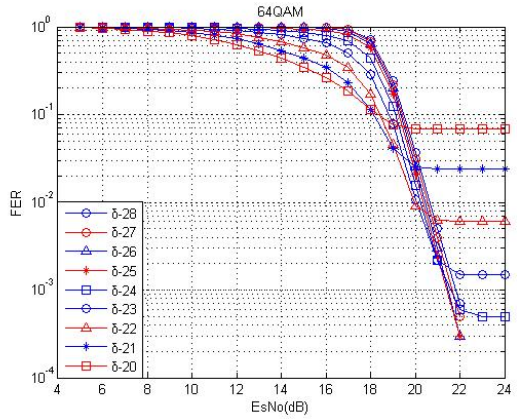
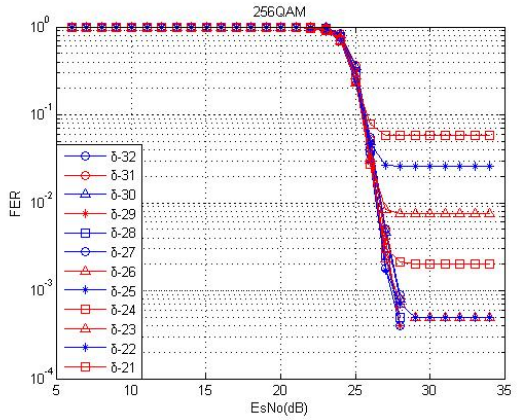


Figure. 2.Model of FEC for CATV down stream channel.



a. 64-QAM



b. 256-QAM

Figure. 3. FER followed by δ

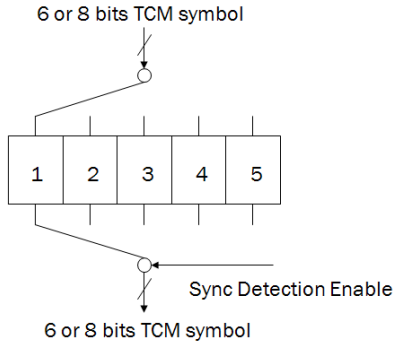


Figure. 4.The 5 register for detection of sync word.

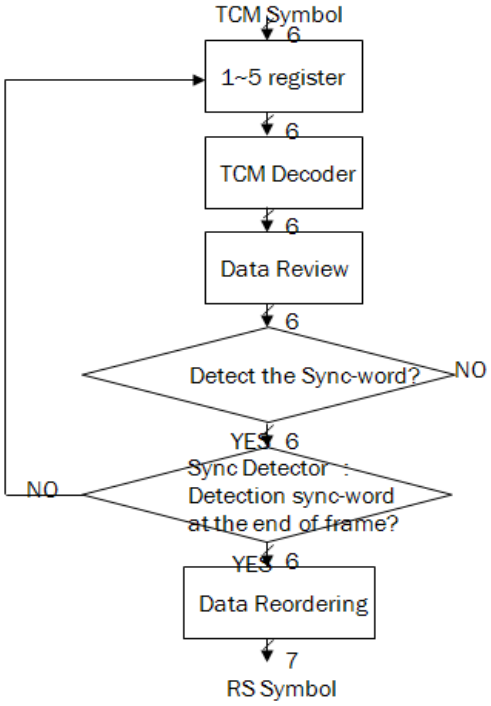


Figure. 5.The 5 register for detection of sync word

4. Problems and Solutions of Implementation

4. 1 Frame synchronization algorithm

As described in Section I, it is very important to find 28-bits sync words for 64- QAM and 38-bits sync word for 256-QAM. In addition, it is also key point demodulated symbols are synchronized to the punctured pattern in TCM decoding process. If demodulated symbols does not synchronized to punctured coded pattern that is branch coded word in trellis diagram, we could not find frame synchronization pattern which provide synchronized e-RS decoding, de-interleaving, de-randomizing.

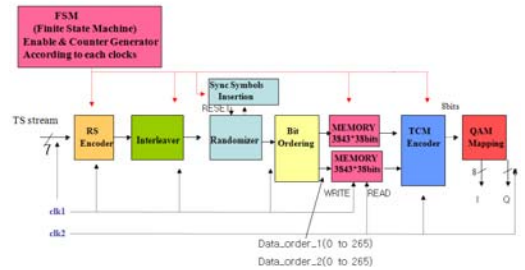
It is easy to find sync word because it's pattern is unique in the FEC frame. However, it is possible there are same sync pattern in each frame in noise channel. Therefore, if we compare exact sync pattern with received symbols, so many frames would be lost. In this paper, we proposed optimal threshold of value of sync word detection. The threshold is described by the following Equation.

$$\delta = \sum_{i=0}^{N_s-1} s_i \oplus s_i \qquad (1)$$

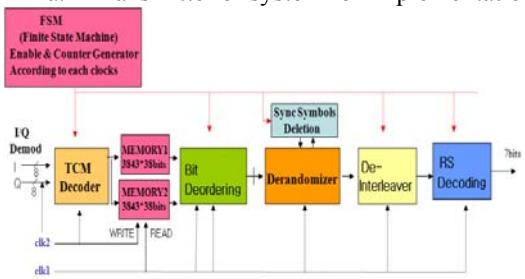
Where, N_s is length of sync word, s_i is i^{th} sync pattern bit, and a_i is i^{th} received decoded bit in the TCM decoder.
Figure. 3 shows the FER(Frame Error Rate) performance in according to δ in 64-QAM and 256-QAM mode. In 64-QAM mode, we have to δ set to more than 24. Otherwise, it occurred error floor because there are same sync patterns in the data fields of a FEC frame. In a similar way, δ must be set to more than 25 in 256-QAM mode.
The length of punctured pattern is spanned to within five QAM symbols. Therefore, this paper propose the sync-word detection algorithm using a simple 5-stage register and FEC frame sync trailer to solve the punctured coded pattern synchronization and frame synchronization together. As shown in Figure. 4, the structure of 5-stage register and flow chart of frame synchronization. The demodulated symbols are buffered in 5-stage FIFO(First In First Out) register. The buffered symbol in first stage register is inputted to TCM decoder. After decoder has been finished the one frame, we checked the 28-bits or 38-bit sync words. If sync words are not found, we moved next stage register to input to decoder.
The Fig. 12 is flow chart of sync word detection.

4. 2 Reduced number of clocks

This system needs different clock at each system block because of different code rate and different modulation type. As shown in Figure. 6, to reduce the number of clocks, we use the two memories, which are different clock speed for reading and writing data.
For the solution of this problem, we used two memories. This is shown in Figure. 6.



a. Transmitter of system for implementation



b. Receiver of system for implementation

Figure. 6.The structure of system for implementation used two memories.

5. Implementation

In this system, we present the cable modem described as section II and section III. We implemented the flexible cable modem using a very high-speed hardware description language (VHDL) and verified its operation by register transfer level (RTL) simulation. The cable modem implemented in VHDL was synthesized for the Xilinx FPGA commercial chip (Vertex II Pro xc2vp30-5) with three million gates as shown in Figure. 7.
The results of timing simulation shown in Figure. 8 are transmitter and receiver. The operating clock speed is 24M sym/sec.

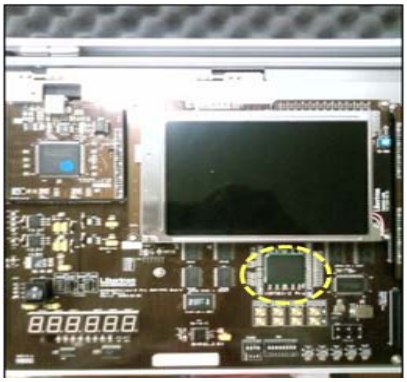
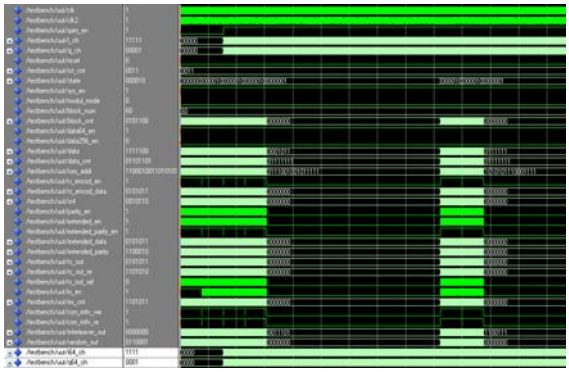
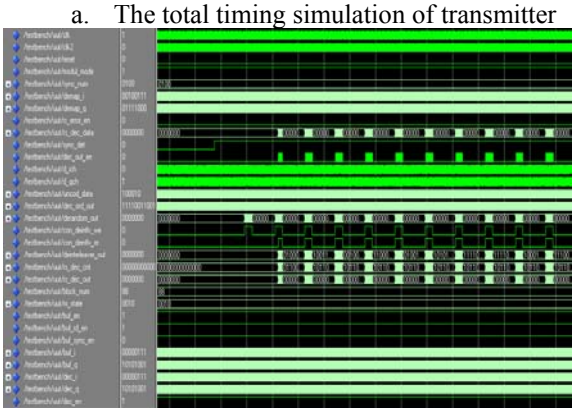


Figure. 7.The FPGA chip (Vertex II Pro c2vp30-5) used implementation.



a. The total timing simulation of transmitter



b. The total timing simulation of receiver

Figure. 8.The total timing simulation of transmitter and receiver.

6. Conclusion

In this paper, we described the performance analysis and design methodology of serial concatenate of extended RS code, trellis coded modulation with 64-/256-QAM, based upon testing and characterization of cable systems in the ITU-T Recommendation J-38 Annex B system. We present two problems in aspect to FPGA implementation. First is synchronization problem of demodulated symbol with puncturing patterns and frame sync words. If demodulated symbols does not synchronized to punctured coded pattern that is branch coded word in trellis diagram, we could not find frame synchronization pattern which provide synchronized e-RS decoding, de-interleaving, de-randomizing. This paper propose the sync-word detection algorithm using a simple 5-stage register and FEC frame sync trailer to solve the punctured coded pattern synchronization and frame synchronization together. Furthermore, we present optimal threshold of sync word dection value in mode of 64-QAM and 256-QAM. Second, many clocks are needed in the transceiver because different coding rate, modulation types, sync bite insertion, and bits to byte conversion. We proposed the effective H/W architecture in implementing FPGA chip by using the two memories which makes using the just one clock.

Based on the solutions, this paper provides effective design methodology of cable transmission systems without an any performance loss and a H/W complexity increasement. Furthermore, it is more applicable to other wireless system which has serial concatenate coded scheme.

Finally, in this paper, we have total timing simulation of system by Modelsim (Xilinx VHDL tool). And we use FPGA chip for the implementation. The chip is 'Vertex II Pro xc2vp30-5' by Xilinx.

References

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[3] G. Ungerboeck, "Trellis Coded Modulation with Redundant Signal Sets, Part II : Introduction" , IEEE Communications Magazine, Vol. 25, No. 2, pp. 12-21, February 1987.