Low Power Consumption Level Shifter Using LTPS TFTs for System-On-Panel

Eun-Woo Jeong and Oh-Kyong Kwon*
Division of Electrical and Computer Engineering, Hanyang University
17 Haengdang-Dong, Seongdong-gu, Seoul, 133-791, Korea
E-mail: okwon@hanyang.ac.kr*

Abstract: A capacitive coupling type level shifter for low power consumption using low temperature poly-Si(LTPS) TFTs is proposed. The concept of the proposed level shifter is to use capacitive coupling effect to reduce short circuit current and power consumption. The fast switching characteristic of capacitive coupling effect reduces the short circuit current during the transition time of input signal. By simulation results, it is verified that the power consumption of the proposed level shifter is reduced up to 53 %, compared to that of the previously reported cross-coupled latch type level shifter.

1. Introduction

Recently the market for portable devices such as PDA or hand-held phone has grown. These devices require display systems with compact size, high quality image, low power consumption and low cost. Low **Temperature** Polycrystalline Silicon (LTPS) technology attracts attention for its potential to integrate the driver circuits and the power management circuits with pixel array on a glass panel[1][2][3]. But power management circuits which are integrated in LTPS panel suffer from low efficiency and difficulty in integrating analog circuit such as regulation; LPTS TFT has some inferior electrical characteristics to single crystalline silicon transistor, which have low mobility, high threshold voltage and non-uniformity of their electrical properties.

Level shifter circuits transfer low-voltage signal to the high-voltage signal in the system. Driving an active matrix LCD display requires relatively high supply voltages between 8 to 15voltage. Since voltage level for logic high is around 5 volts, it is necessary to amplify the magnitude at the last stage of LCD driving circuits by using the level shifter.

Level shifter need have more high speed performance and more low power consumption, because the number of level shifter in data driver circuits is increased due to its increasing output channel and the operating frequency is increased due to higher resolution.

Therefore, we proposed the new level shifter circuit, which has high operating speed and low power consumption, using LTPS TFTs that have low mobility and high threshold voltage.

2. Conventional level shifter

Figure 1 shows the schematic diagram of a previoulsy reported cross-coupled latch type level shifter where inputs low supply voltage and the output high supply voltage VDDH are used.

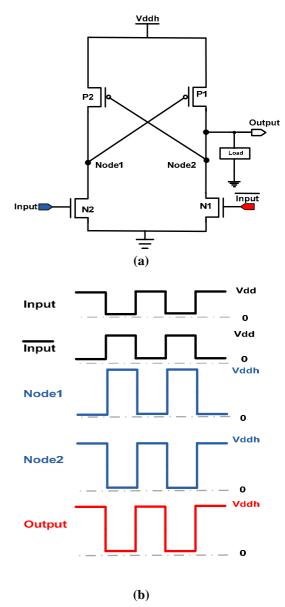


Figure 1. The previously reported cross-coupled latch type level shifter: (a) schematic diagram and (b) driving waveforms.

This level shifter consist of 2 p-type TFT and 2 n-type TFT. The two p-type TFT P1 and P2 act as a cross-coupled load. Using the positive and the negative of input low level voltage input signal. Thus, input signal control the turn-on and turn-off state of the n-type TFT (N1,N2). This level shifter have high power consumption because p-type TFT gate voltage between VDDH to GND during passes short circuit current[4].

Therefore, we proposed a new capacitive coupling type level shifter, which decreases power consumption by decreasing short circuit current.

3. The proposed level shifter

Figure 2 shows the schematic diagram of the proposed capacitive coupling type level shifter which can solve power consumption problems of the previously reported latch type level shifter circuits using LTPS TFTs. As shown in the figure 2, the proposed circuit is composed of three p-type TFTs and two n-type TFTs and one capacitor.

Driving waveforms of the proposed level shifter are shown in figure 2(b). In the first phase, when the input signal is 'High', the voltage at node1 rises to 2VDD and turns off the P2 TFT and turn on N2 TFT and the node2 is dischareged to GND. Correspondingly, the voltage at node2 turns on the P1 TFT. At the same time, P3 TFT is turned off by setting the gate voltage of the output voltage 'VDDH' and N1 TFT is turned off by input signal becomes 'Low'.

In the second phase, when the input signal becomes 'Low', the node1 voltage changes from 2VDD to VDD, and the N1 TFT is turned on. As a result P2 TFT is turn on, node2 voltage changes from GND to VDDH. The P1 TFT and the N2 TFT are turned off at the same time. This operation principle is symmetrical as explained in the case of the opposite phase of the input signals.

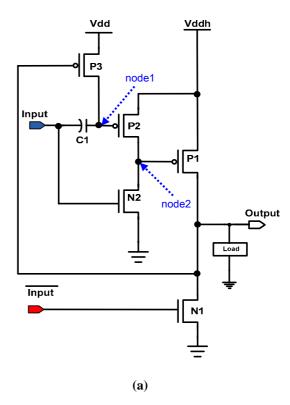
As a result, the proposed circuit has fast switching characteristic of capacitive coupling effect, which reduces the short circuit current during the transition time of input signal.

4. Simulation results

We simulated the performance of the previously reported and the proposed circuits using HSPICE. We assume that the input voltage is 5V, and that a display system is QVGA poly- Si TFT LCD panel in which driver circuits and power circuits are integrated and that the VDDH is 10V.

Table 1. Simulation condition of the previous and the proposed level shifter

Display format	QVGA
Input signal level (VDD)	5V
Output signal level (VDDH)	10V
C_{load}	50 fF



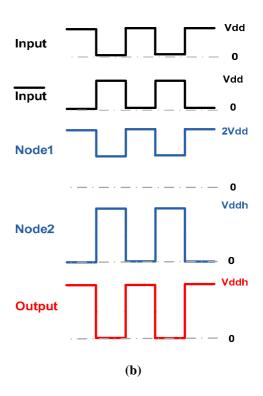


Figure 2. The proposed level shifter: (a) Schematic diagram and (b) driving waveforms.

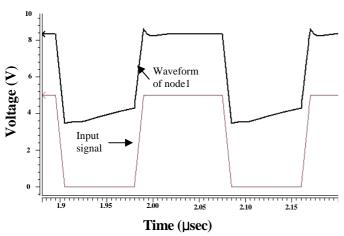


Figure 3. Simulated waveforms of node1 of the proposed level shifter

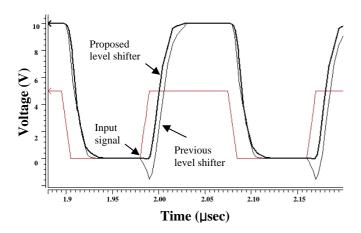


Figure 4. Simulated output waveforms of previous reported and the proposed level shifter

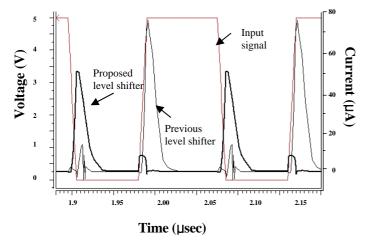


Figure 5. Simulated current waveforms (N1 TFT) of previous reported and the proposed level shifter.

Figure 3 shows the simulated waveform of node1 in the proposed circuit. We can confirm that the proposed circuit operates capcitve coupled type level shifter.

Table 2. Simulation results of the proposed level shifter and previously reported level shifter

	Previously reported circuit	Proposed circuit
Power consumption (mW)	169	80
Delay(ns)	16	10
Short circuit current Max (µA)	80	55

Figure 4 shows the simulated output voltage waveforms of driving TFT of the previous reported and the proposed circuits. We found that proposed level shifter is superior to conventional level shifter in terms of speed. Figure 5 shows the simulated current waveforms of N1 TFT source of the previous reported and the proposed circuits.

As shown in the figure 5, short circuit current of the proposed level shifter was decreased by 32% with respect to the previous one. Table 2 compares the efficiency of previous circuit and proposed circuit which are obtained by simulation.

As shown in table 2, the proposed level shifter circuit has 53% power consumption reduction and delay decrease 47% compared to the conventional level shifter.

5. Conclusions

We proposed a new level shifter circuits suitable for LTPS TFT technology. We analyzed two kinds of level shifter at first: the conventional level shifter and proposed a new level shifter. Then we proposed a new level shifter with lower power consumption. Because fast switching characteristic of capacitive coupling effect reduces the short circuit current during the transition time of input signal. By simulation results, it is verified that the power consumption of the proposed level shifter is reduced up to 53 %. It shows that the proposed level shifter can be applicable for mobile technology such as low power consumption.

References

- [1] S.-S. Han, K.-M. Lim and C.-D. Kim, "3.5 inch QVGA Low Temperature Poly-Si TFT LCD with Integrated Driver Circuits," *SID Technical Digest*, pp. 208-211, 2003.
- [2] N. Toyozawa, Y. Nakajima, H. Yoshine, S. Noichi, K. Yuda, S. Toriyama, A. Ogawa, T. Yoshikawa and Y. Maki, "Low-Power Integrated Circuit Technologies Using Low Temperature Poly-Si TFTs for Mobile Device Applications," SID Technical Digest, pp. 686-689, 2002.

- [3] J.-Y. Choi, B.-C. Cho, H.-S. Sim and O.-K. Kwon, "A New DC-DC Converter for Gate Driver Circuit Using Low Temperature Poly-Si TFT," *IMID Technical Digest*, pp. 116-119, 2004.
- [4] H.-S. Shim, J.-H. Kim, B.-C. Cho and O.-K. Kwon, "A New Level Shifter Using Low Temperature Poly-Si TFTs," *IMID Technical Digest*, pp. 117-120, 2003.