The Design of TFT-LCD Source Driver using Offset Cancellation Method by High Frequency Modulation and Layout Scheme

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Abstract: In this paper, a dynamic offset cancellation method using simple high frequency modulation has been proposed, designed and verified with SPICE simulation. It was realized the 8-bit source driver channel structure layout using the proposed layout scheme. The proposed offset cancellation method can realized low offset compared to the conventional method. The offset voltages of differential amplifiers with same input signal can be modulated from DC to the KHz frequency region in the conventional method but proposed method can be modulated from DC to the MHz frequency region. After modulation is performed through low pass filtering, the error voltage magnitude can be minimized to the level of sub mV. Also the output glitches normally associated with "hand-over" events by some switching operation can be attenuated by the proposed method. HSPICE simulation using 0.3-μm 18-V high voltage CMOS process parameters to verify the performance of proposed method is extensively performed and shows an input-referred offset variation of less than 1mV and hand-over glitches below 5mV.

1. Introduction

To driving the column of *TFT-LCD* with high color depth above *8-bit*, *OP-amps* with very high voltage accuracy less than 1mV is needed. But the realization of low offset op-amp to drive *TFT-LCD* source is significantly difficult. This is the most important technical issue in designing *OP-Amps*. In *OP-Amps* design, mostly, the offset of *OP-Amps* is composed as the systematic offset and the random offset [1].

Because systematic offset is very small, the major concern of offset is random offset by semiconductor manufacturing process variations, like etching, diffusion, oxide thickness variation. The most part of random offset in the conventional *OP-Amps* as shown in Figure 1, occurs by the process variations. For example, the size mismatch and threshold voltage mismatch between *MN1* and *MN2*, *MP1* and *MP2* are the major factor.

In *TFT-LCD* column driving, small sized *OP-Amp* with sub-mV offset is the most important design issues and generally to get the desired low offset voltage, the method of increasing the dimension of critically matched *CMOS* transistors is simply applied. But this is not practical in sides of cost and mass production. For this reason, the need for *OP-Amps* with small sized but very low random offset is increasing as time goes by.

In this paper, we present a simple chopper type dynamic offset cancellation method with dual differential amplifiers in realizing *OP-Amp*, some switches for modulating dc offset voltage and output driver stage for reducing effectively the random offset.

In section 2 and section 3, the previous and proposed offset cancellation method are explained. Experimental results are demonstrated in section 4 and conclusions in Section 5.

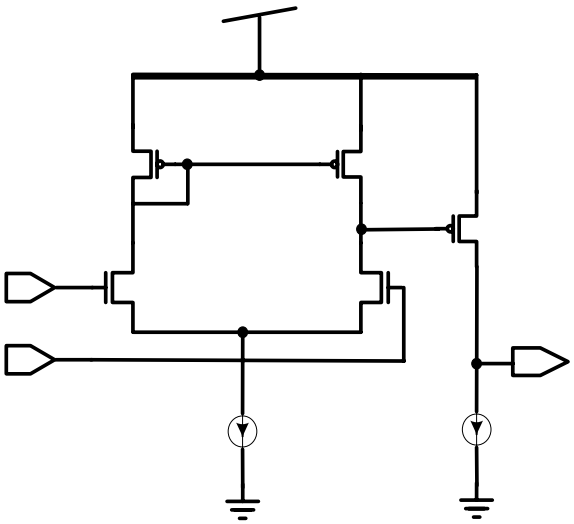

Figure 1. The differential amplifier circuit

2. Previous offset-cancellation method

Previous dynamic offset cancellation techniques normally fall in two categories, auto-zeroing or chopper-stabilized, which are based on sampling and modulation principles, respectively. In basic form, the auto-zeroing scheme only processes the input signal half of the time and is not continuous. *CHS* techniques, on the other hand, are not only continuous but also band limited, since the frequency of the input signal must be less than half the chopping frequency (to prevent aliasing). What is more, the chopping frequency cannot exceed several tens of kHz because of switch charge injection non idealities, limiting them to low bandwidth applications. However, combining the attributes of auto-zeroing with ping-pong constitute a viable solution for continuous low-offset operation with minimal constraints on signal bandwidth [2].

a. Auto-Zeroing Method (*AZ*)

The basic idea of *AZ* is sampling the unwanted quantity (noise and offset) and then subtracting it from the instantaneous value of the contaminated signal either at the input or the output of the op-amp. This cancellation can

also be done at some intermediate node between the input and the output of the op-amp, using an additional input port defined as the null input and identified with the Amp in the schematics of Figure 2 [2].

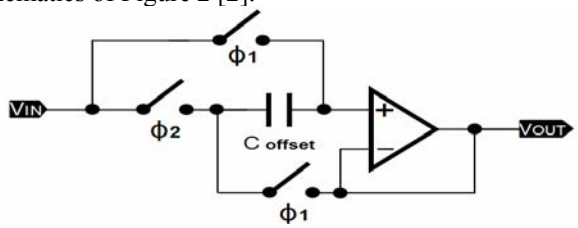

Figure 2. Auto-Zeroing method block diagram

b. Chopper Stabilization Method (*CHS*)

CHS technique was introduced about 50 years ago to realize high-precision dc gains with ac-coupled amplifiers. These were originally constructed using vacuum tubes and mechanical relay choppers. When solid-state components became available, they were then made with modular and hybrid techniques. Now they can easily be realized on-chip by taking advantage of integrated switches [2].

Unlike the *AZ* process, the *CHS* technique does not use sampling, but rather applies modulation to transpose the signal to a higher frequency where there is no l/f noise, and then demodulates it back to the baseband after amplification. The chopper amplification principle is illustrated in Figure 3 [2].

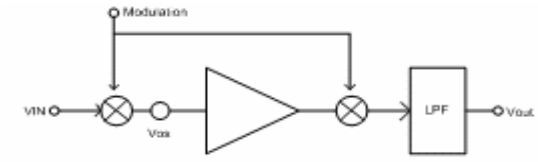

Figure 3. Block diagram of the Chopping method

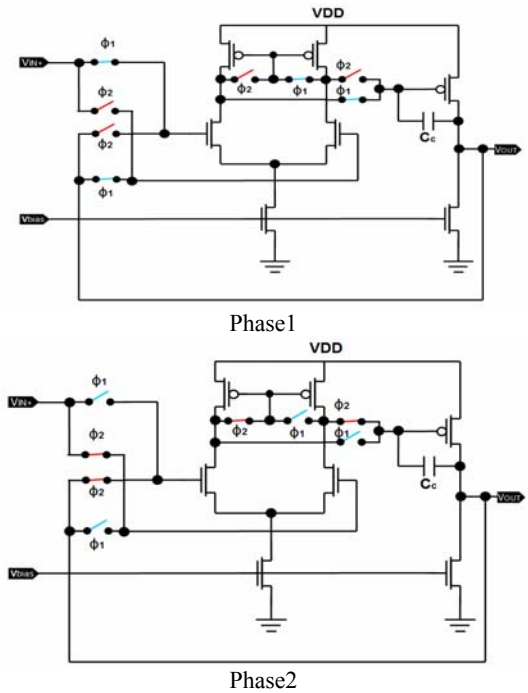

Figure 4. Circuit of Chopping mehtod

The example of *CHS* technique is shown in *Figure. 4*. This scheme is the fundamental scheme for modulating random dc offset to move up to high frequency region by repeating the sequence *Phase1* and *Phase2* state with regular cycle. By using this method, random offset can be eliminated.

But this type of offset cancellation method has two of significant disadvantages. First disadvantage is that too many switches are applied for modulator. So layout area by switches is not ignorable in these days. And second disadvantage is that the modulation frequency is limited to very low frequency. As a result, the random offset can not be suppressed sufficiently to the acceptable offset voltage level.

3. Proposed offset-cancellation method

In order to decrease the area and random offset, chopper-type amplifier in Figure. 5 is proposed in this paper. Figure 6 shows the propoed dual differential amplifiers and Figure 7 shows the layout arrangements of transistors for reducing the ramdom offset.

Generally, in the case of using single differential amplifier as in Figure 1, the random offset directly affects to output voltage and this random offset can be described as *(1)* [3].

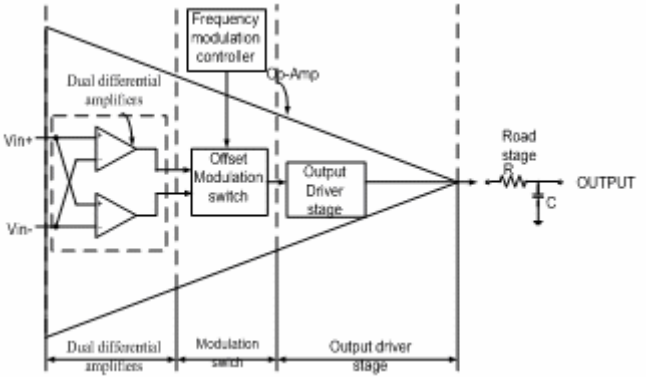

Figure 5. The block diagram of porposed offset cancellation method

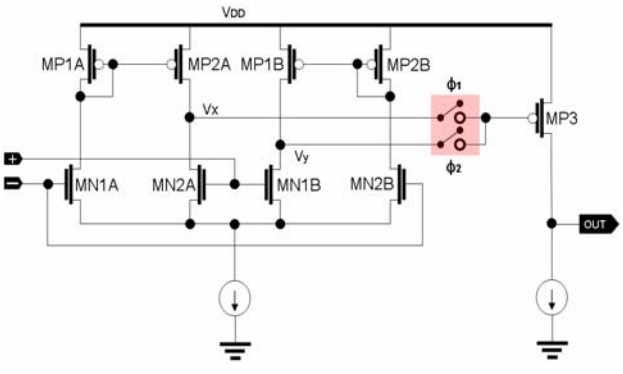

Figure 6. Proposed dual differential amplifier

Therefore if the differential amplifiers in Figure 6 are spatially placed as in Figure 7, error voltage V_x by the mismatch of *MN1A/MN2A* and that of V_y by the mismatch of *MN1B/MN2B* will be the one of *CASE A* or *CASE B* as

shown in Figure 8. V_{OSA} is the offset by V_X and V_{OSB} is the offset by V_y and V_{OS} is the offset by V_{exp}. This can be realized with using high frequency modulator in Figure 5. *OP-Amp* output offset will be determined by *(1)* and *(2)*. Finally, the average value of V_{OSA} and V_{OSB} in the proposed offset cancellation method will be same with V_{OS} as in *(3)*.

$$V_{OSA}=V_{GSN,2A}+V_{GSP,2A}\frac{g_{mP,2A}}{g_{mN,2A}}+\frac{(V_{GS}-V_{th})_{N1,2A}}{2}\left[-\frac{\Delta(W/L)_{N1,2A}}{(W/L)_{N1,2A}}+\frac{\Delta(W/L)_{P1,2A}}{(W/L)_{P1,2A}}\right]+\frac{\Delta V_{GSB}}{A_{vdin}} \quad (1)$$

$$V_{OSB}=V_{GSN,2B}+V_{GSP,2B}\frac{g_{mP,2B}}{g_{mN,2B}}+\frac{(V_{GS}-V_{th})_{N1,2B}}{2}\left[-\frac{\Delta(W/L)_{N1,2B}}{(W/L)_{N1,2B}}+\frac{\Delta(W/L)_{P1,2B}}{(W/L)_{P1,2B}}\right]+\frac{\Delta V_{GSB}}{A_{vdin}} \quad (2)$$

$$V_{OS}=\frac{V_{OSA}+V_{OSB}}{2} \quad (3)$$

4. Simulation Results

In order to investigate the offset cancellation, it is needed to have an assumption, that the mismatch ratio between left stage and right stage in Figure 6 should be matched. In layout perspective, Figure 7 will be a good case for matching between two differential amplifiers. *SPICE* simulation condition is summarized in Table 1. Because of this proposed *OP-Amp* will be applied to large *TFT-LCD* column driver *IC* with high voltage supply from *6V* to *17V*, *0.3um 18V* high voltage *CMOS* process parameters are used to verify offset cancellation method.

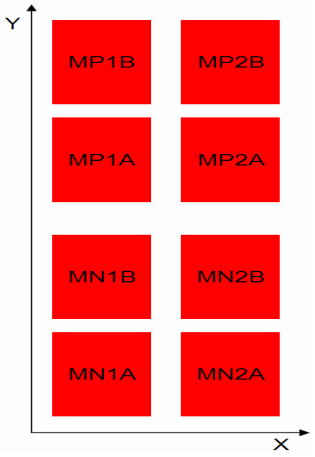

Figure 7. Proposed layout scheme for offeset cancellation

Table 1. Summary of simulation conditions

Items	Conventional OP-Amp.	Proposed OP-Amp.	unit
MN1, MN2	20/9/2	20/9/1	um
MP1, MP2	12/9/2	12/9/1	um
Modulation frequency	30	8M	Hz
Layout Method	Common centriod	Fig.7	
VDD	15		V
Vin	14.8		
Static current consumption	7.5		uA/amp.
R	2		kohm
C	60		pF
technology	0.3um/18V CMOS process		

As in Figure 9, Proposed *OP-Amps* drive *RC* network that means the equivalent load of *TFT-LCD*. Total equivalent R_{total} and C_{total} values are *10kohm* and *300pF* each other.

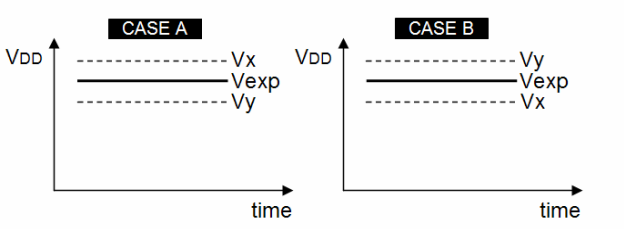

Figure 8. Error voltages by mismatch in Fig.6

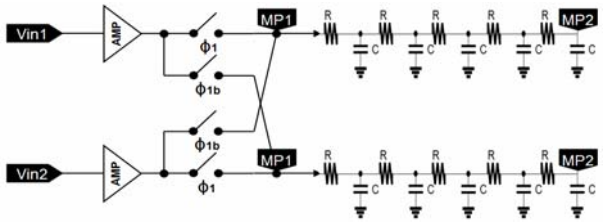

Figure 9. Scheme for SPICE Simulation with typical equivalent RC network of TFT-LCD

Figure 10 is a comparison of output waveform between existing conventional *CHS* and proposed *CHS* for same input. Generally, modulation frequency of existing method depends on the frame rate of *LCD* module. This means that the modulation frequency of existing method is locating at *30Hz* region as shown in Figure 11.

This means that in the case of existing *CHS*, the suppression of error voltage in electrical side doesn't exist. Therefore, the random offset of conventional *OP-Amp* output can be detected by human eyes if the random offset is over *30mV*. But the modulation frequency of proposed *CHS* is not related to frame rate of *LCD* module and can be controlled flexibly by control logic in column driver *IC*. So the error voltage of proposed *OP-Amp* can suppress the error voltage about *-3dB* when *8MHz* modulation frequency is applied. The output waveform shows good offset suppression characteristic under *1mV* at *MP2* of *RC* network as in Figure 10. Figure 12 shows the layout arrangement using proposed transistor layout scheme. Figure 13 shows the layout arrangement of the 8-bit source driver channel structure.

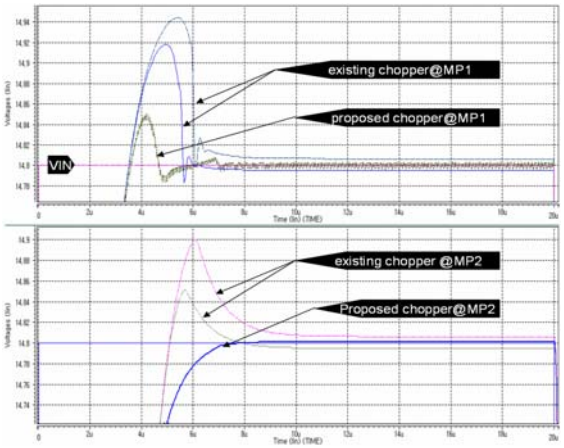

Figure 10. Transient simulation result in Figure 9.

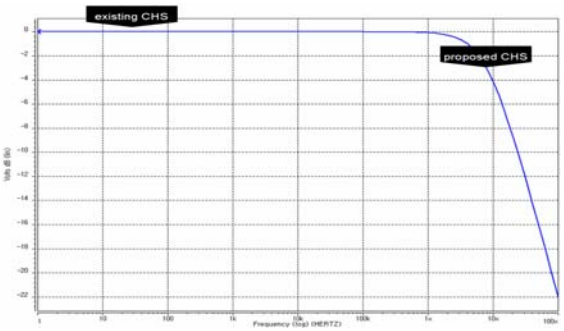

Figure 11. Frequency response of RC LPF (R/C=2kohm/60pF)

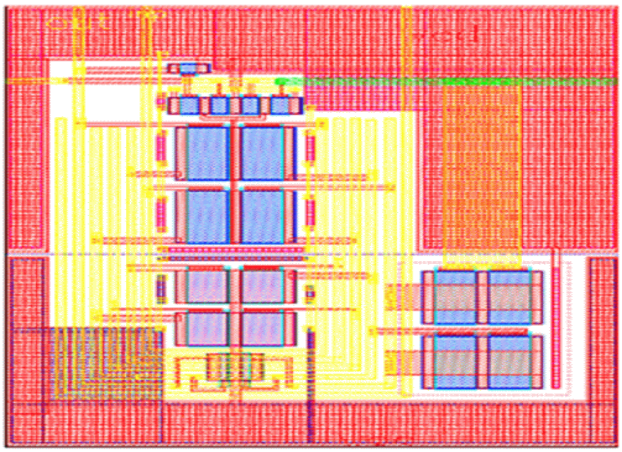

Figure 12. The Layout arrangement for proposed offset cancellation

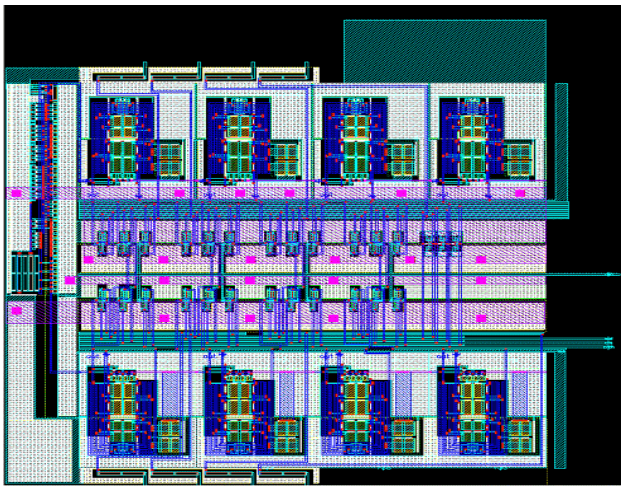

Figure 13. Layout design of 8-bit source driver channel structure

5. Conclusions

A dynamic offset cancellation method using simple high frequency modulation has been proposed, designed and verified with SPICE simulation. The layout of 8-bit source driver channel structure is realized by using the proposed layout scheme. The proposed circuit effectively reduces the systematic offset and the random offset. The total offset is shown under *1mV* and hand-over glitches below *5mV* if the matching of dual differential amplifier stages is perfect. From simulation results, *20mV* offset of the conventional *OP-Amp* could be reduced to under *1mV* by using the proposed method. The measured data shows that the proposed offset cancellation method is very applicable to the design of TFT LCD Source driver. Accordingly, the proposed circuit is suitable for the *OP-Amps* for the column data drivers of *TFT-LCD* with high gray-scale, above *10-bit*. The proposed circuit is also suitable for low offset differential *OP-Amps* because it can reduce the offset of overall circuit. Proposed method in this paper also can reduce the chip size of driver IC with 2-switches but 8-switches in previous method.

6. Acknowledgments

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